

IGT30

Compal confidential

Schematics Document Mobile Merom uFCPGA with Intel Crestline_GM/PM+ICH8-M core logic

Monday, December 25, 2006

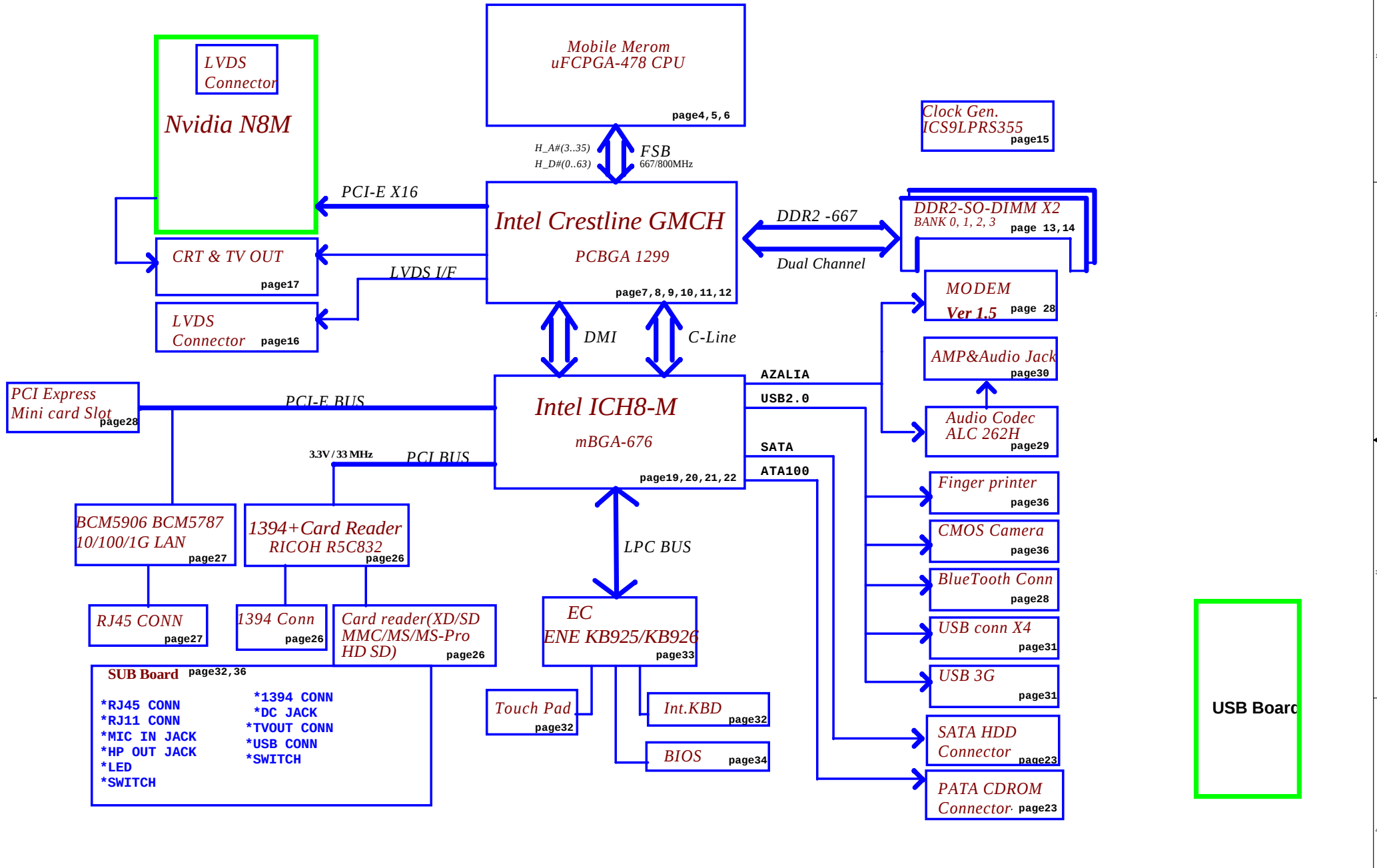
REV:0.1

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LEFT SWITCH Board

LEDs Board



USB Board

TP Board

Voltage Rails

0 MEANS ON X MEANS OFF

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	CLOCK
S0	0	0	0	0	0
S3	0	0	0	X	0
S5 S4/AC	0	0	X	X	0
S5 S4/ Battery only	0	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

ICH8 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Structure

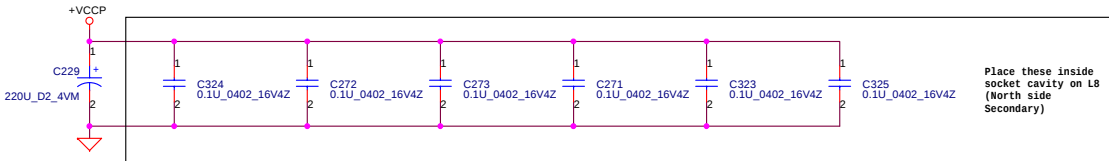
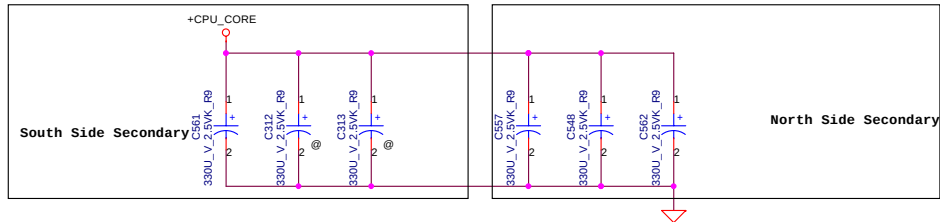
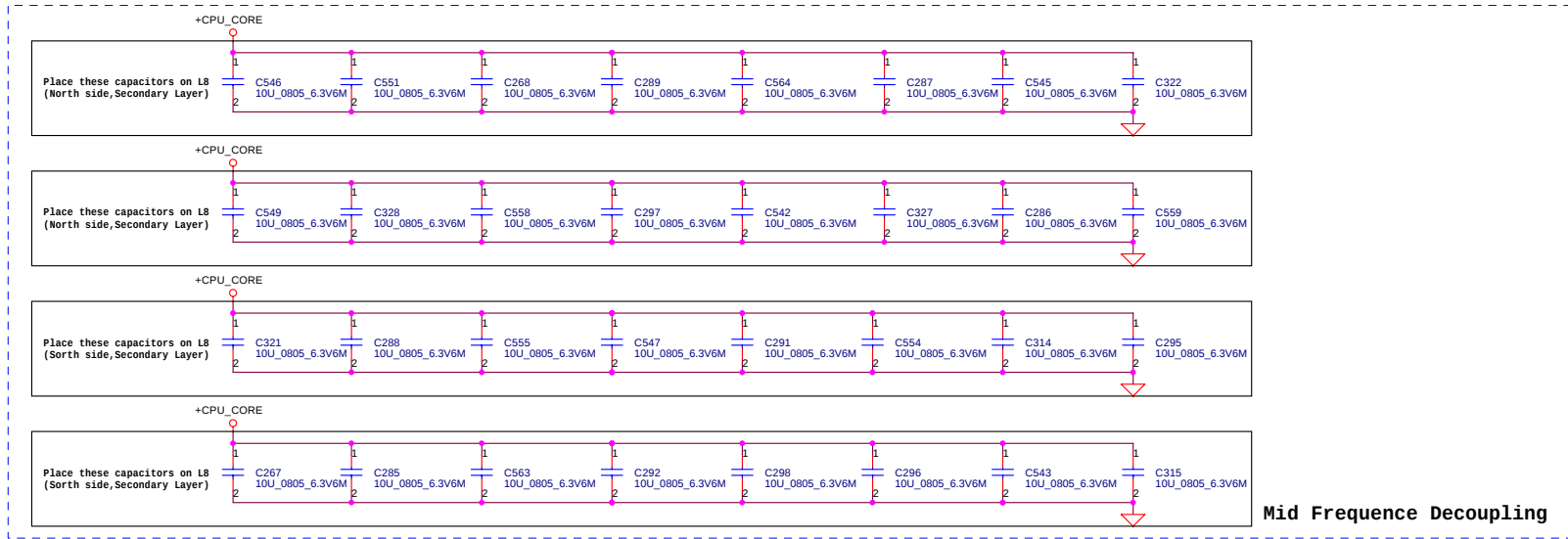
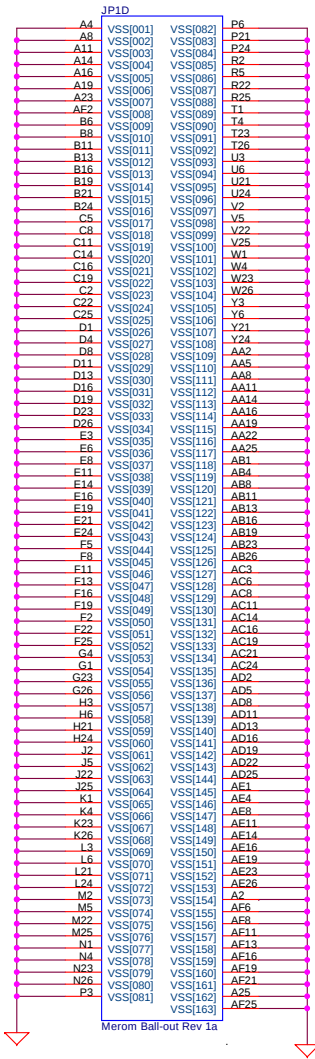
MARK	FUNCTION
@	NC FOR ALL
GIGA@	BCM5787
100@	BCM5906
UMA@	Internal 965GM
VGA@	965PM + Ext VGA

Address

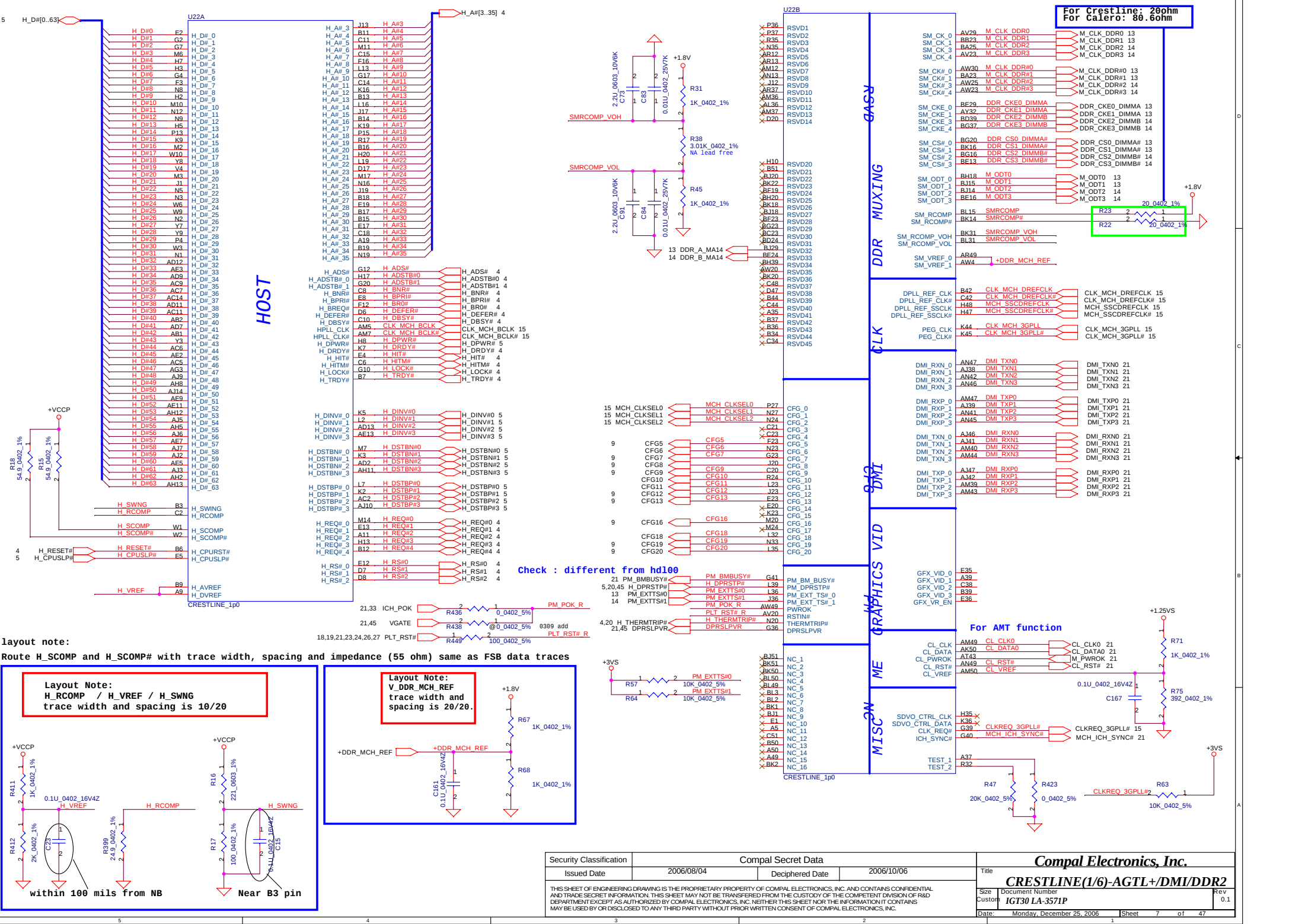
USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	
7	BT(HDL20)
8	
9	3G

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1		47			



layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

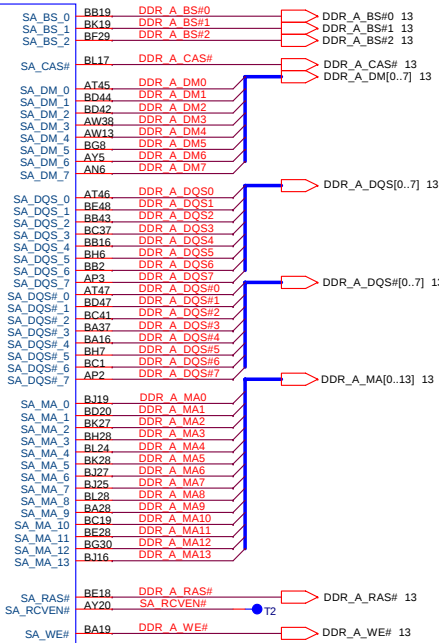
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CRESTLINE(1/6)-AGTL+/DMI/DDR2		Size: 1GT30 LA-3571P	
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13 DDR_A_D[0..63]

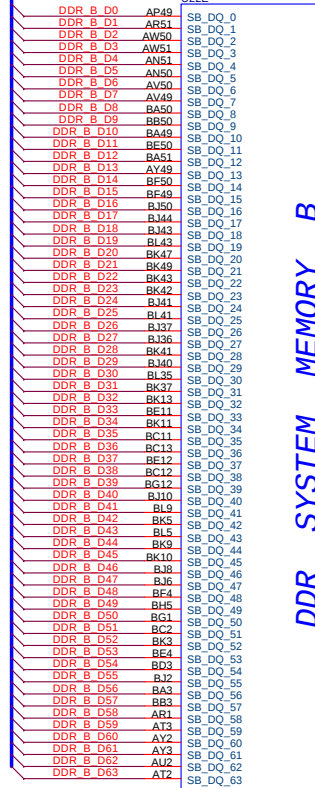


DDR SYSTEM MEMORY A

CRESTLINE_1p0

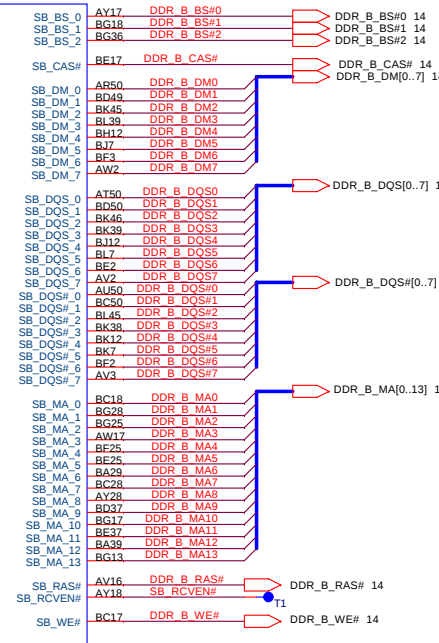


14 DDR_B_D[0..63]



DDR SYSTEM MEMORY B

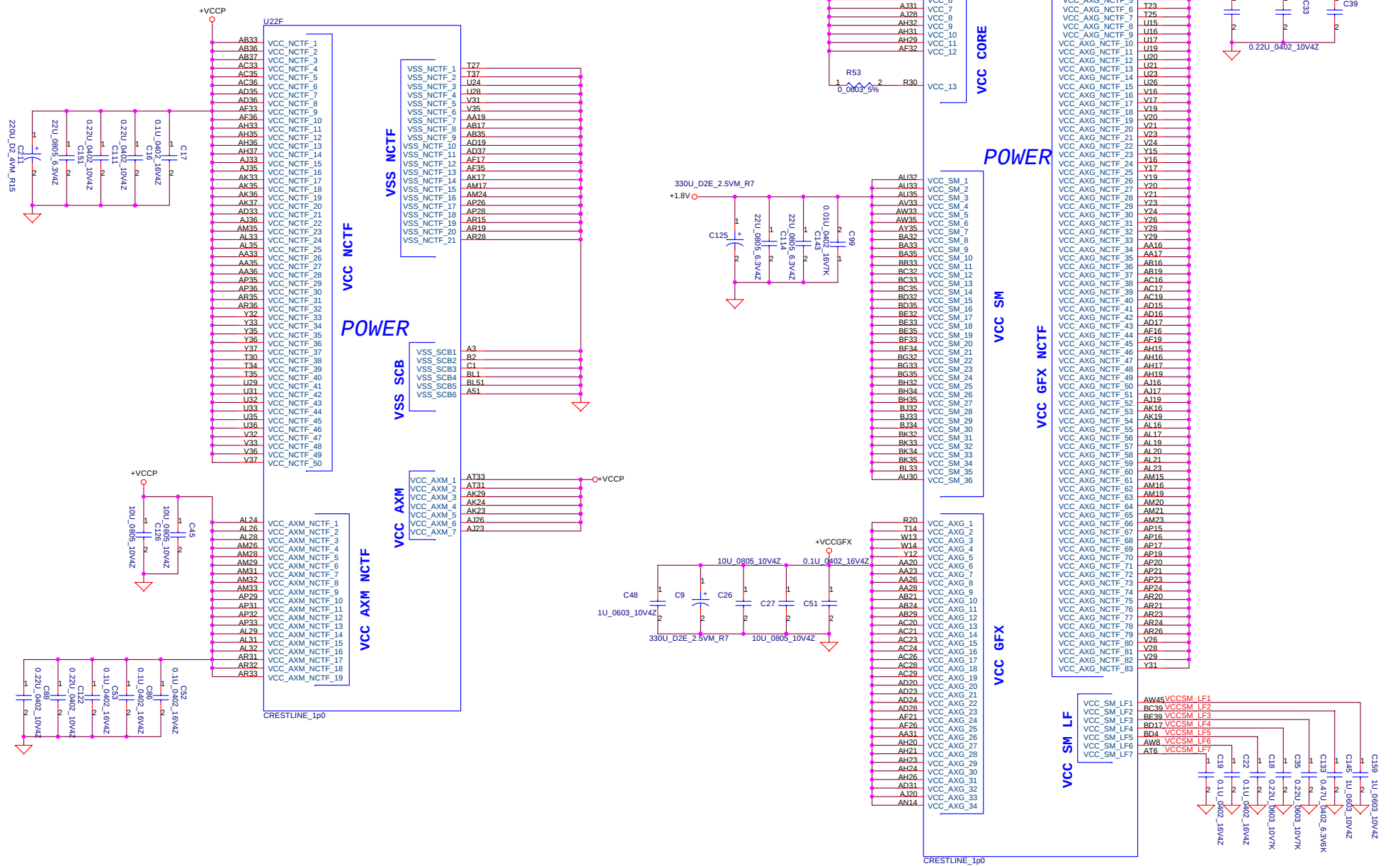
CRESTLINE_1p0



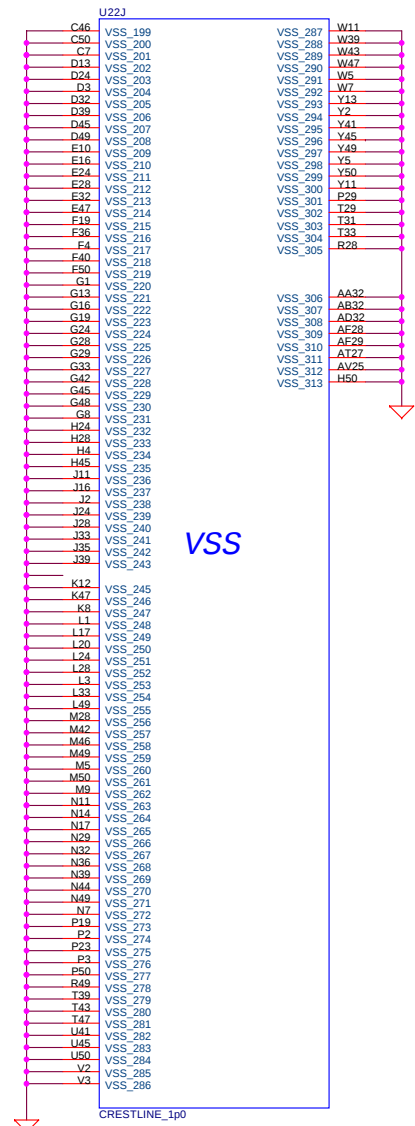
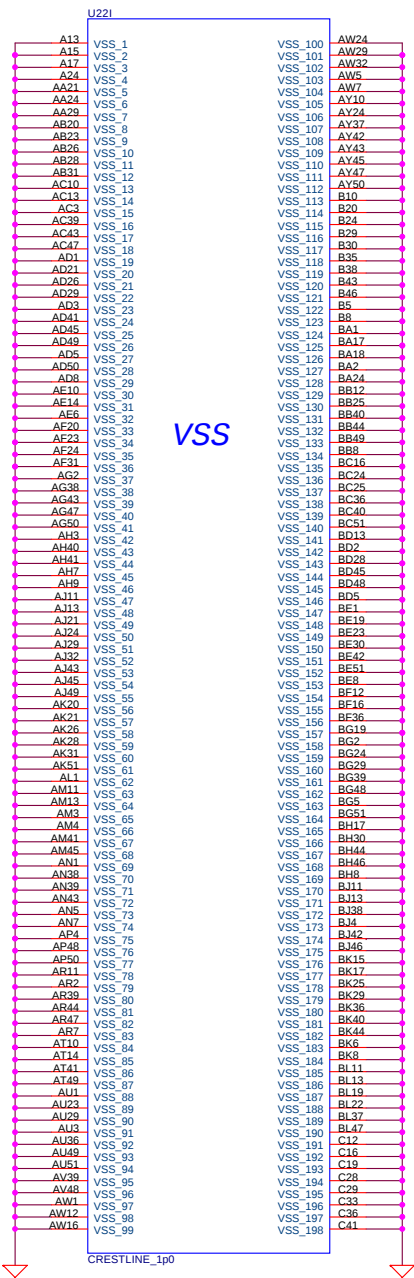
Compal Electronics, Inc.

CRESTLINE((2/6)-DDR2 A/B CH

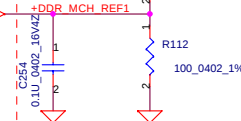
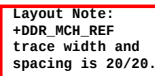
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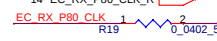
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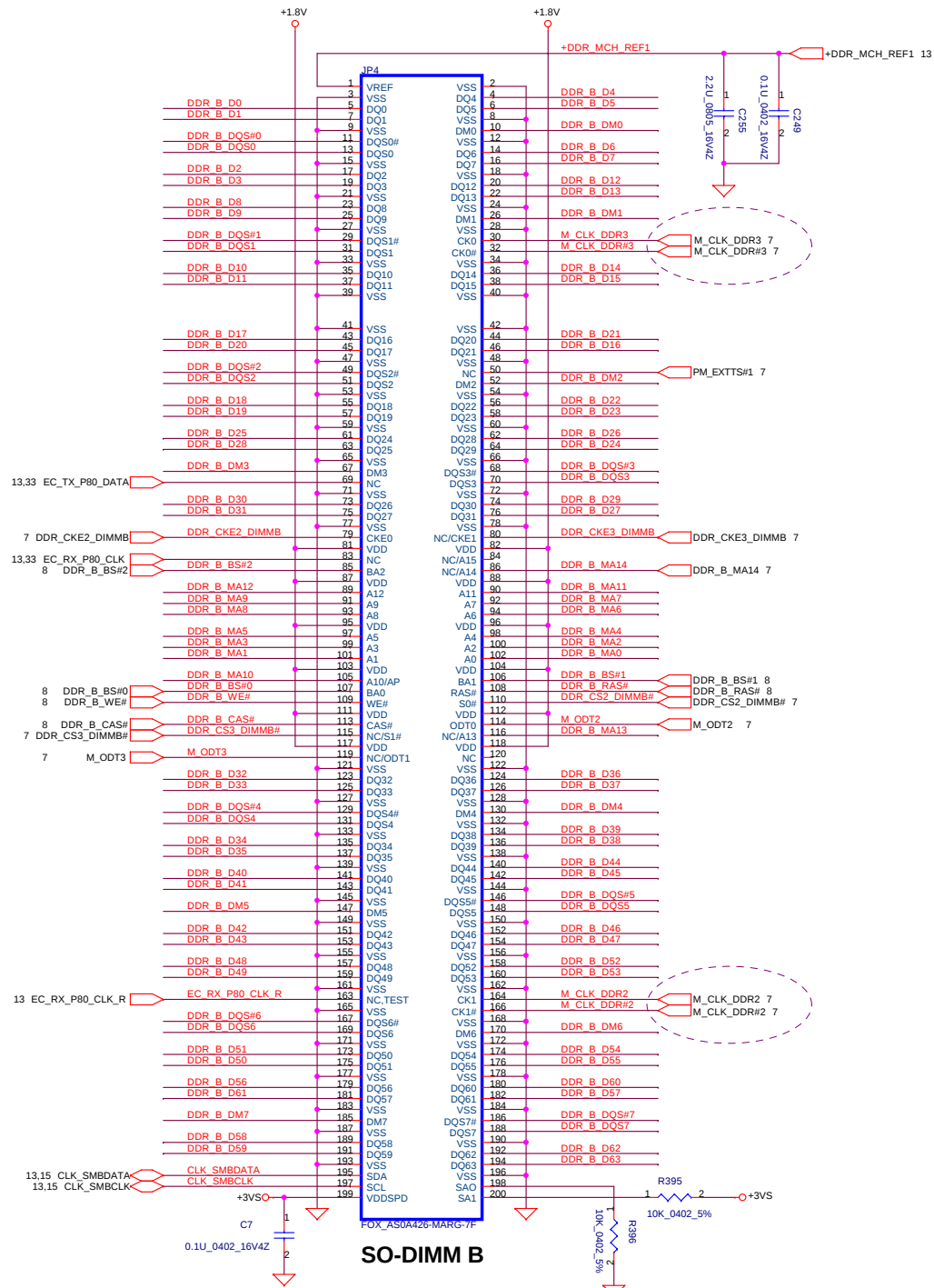
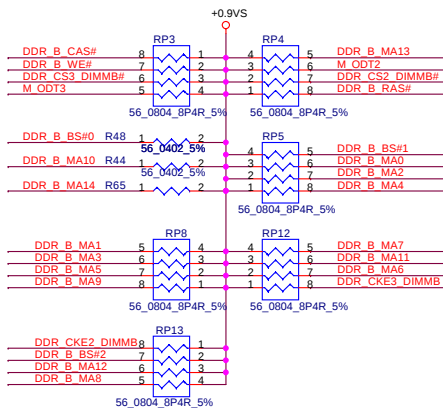
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Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"



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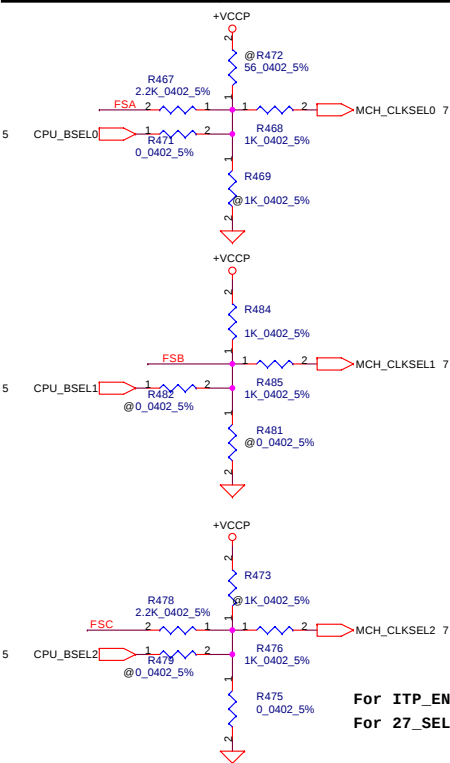


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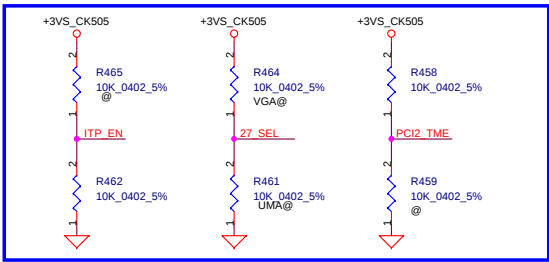
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

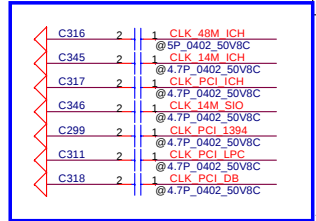
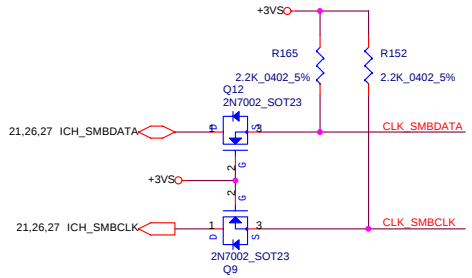
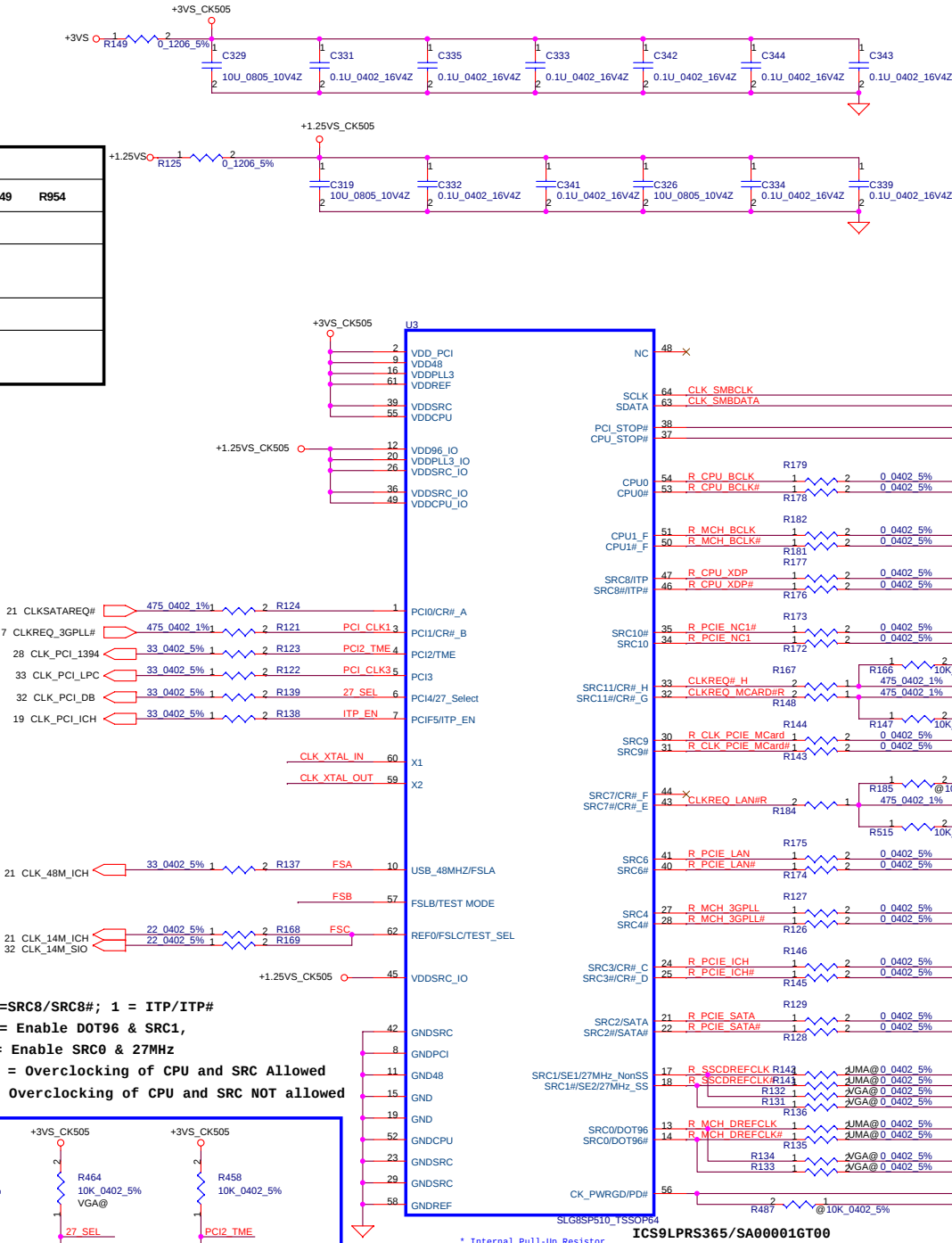
CPU Driven	Stuff	R919	R940	R956
*(Default)	No Stuff	R914	R921	R930
		R943	R949	R954
667MHZ	Stuff	R959	R930	R914
	No Stuff	R919	R940	R956
		R949	R943	R921
800MHZ	Stuff	R959	R930	R921
	No Stuff	R919	R940	R956
		R949	R943	R914



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

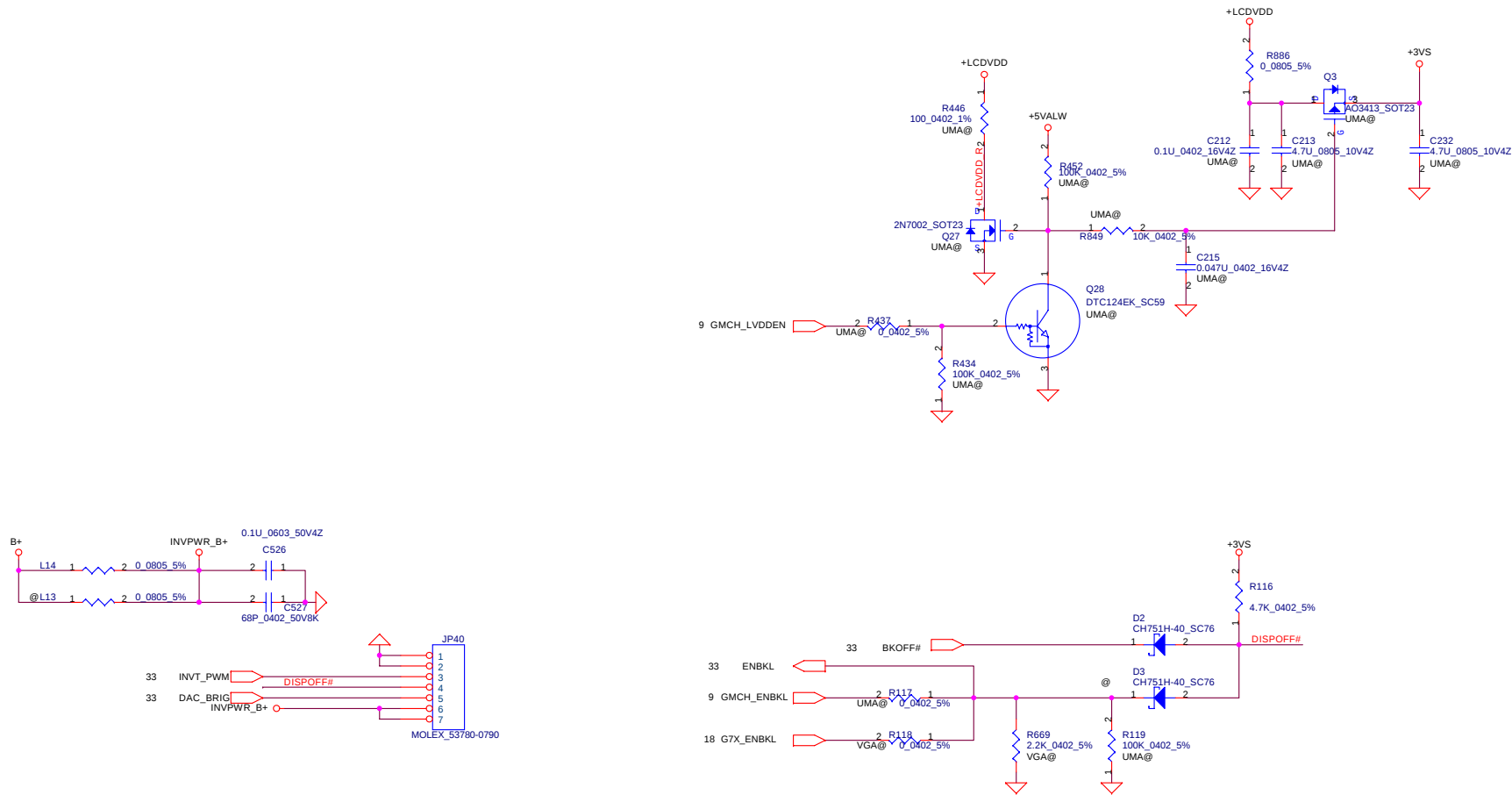


Routing the trace at least 10mil

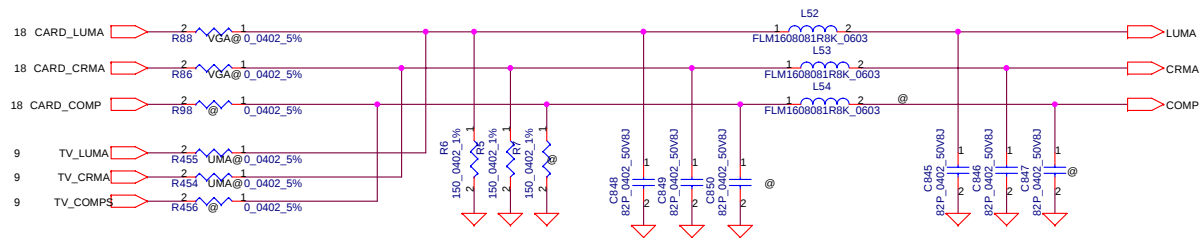


Place close to U41

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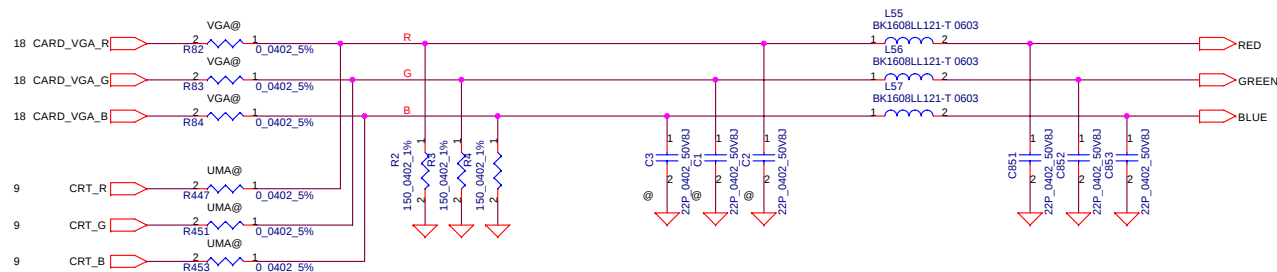


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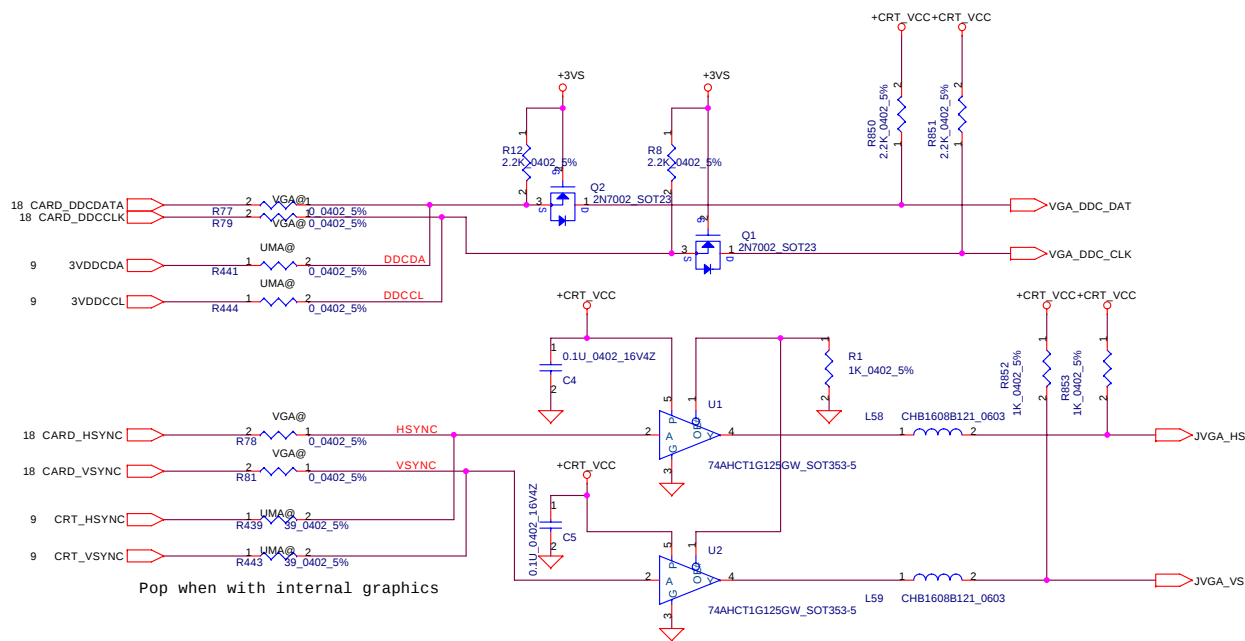


Pop when with internal graphics

CRT Conn.



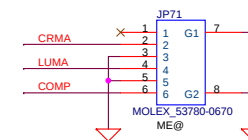
Pop when with internal graphics



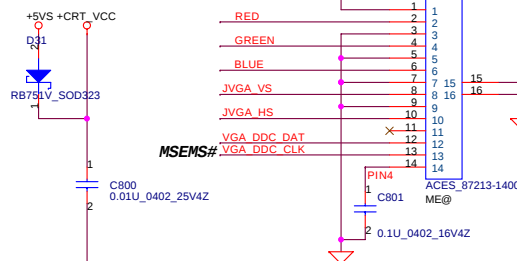
Pop when with internal graphics

VGA I/O PORT Connector

S-VIDEO

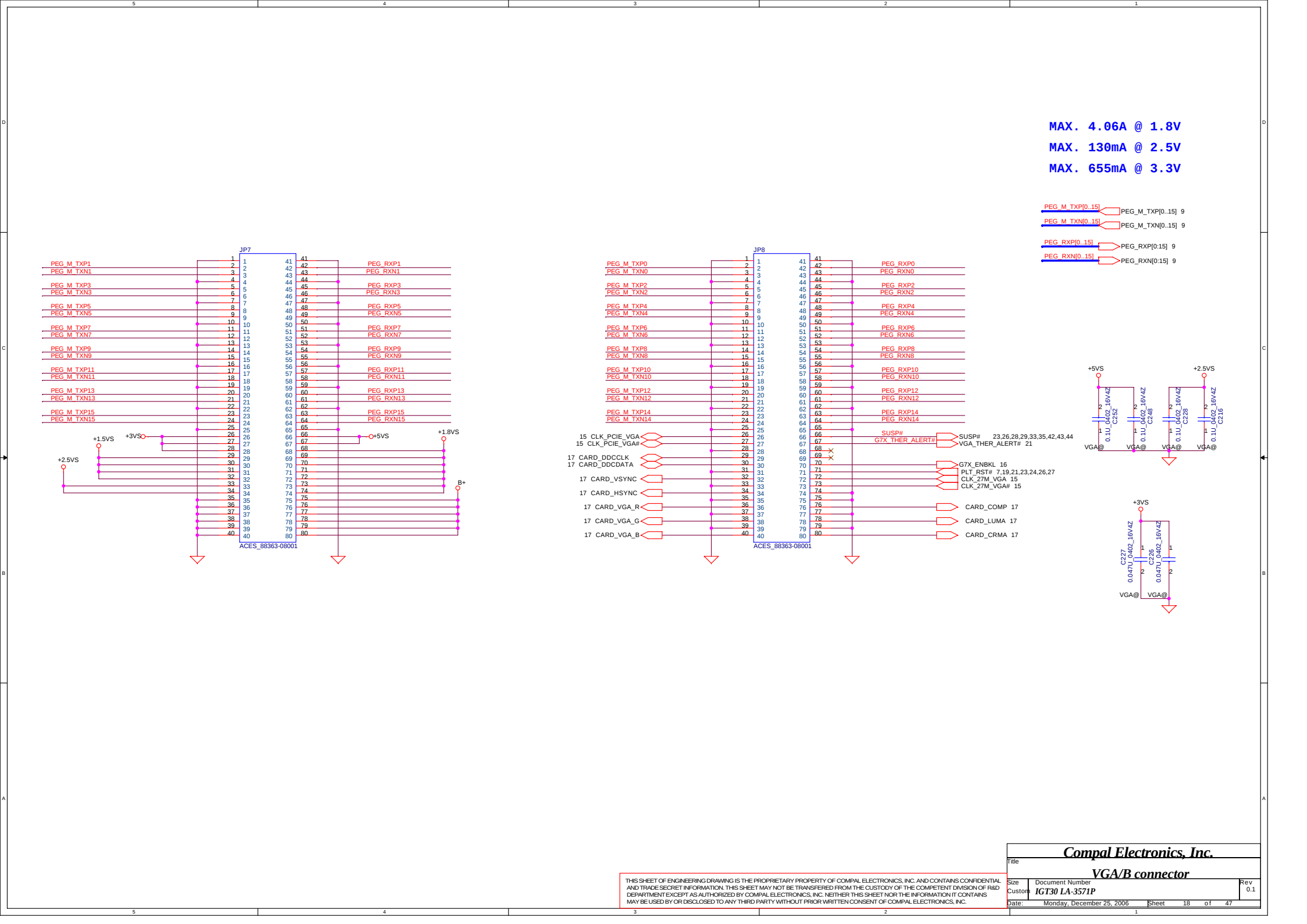


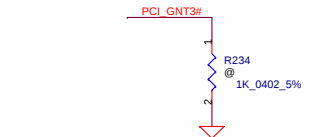
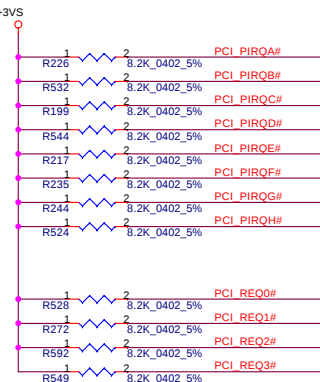
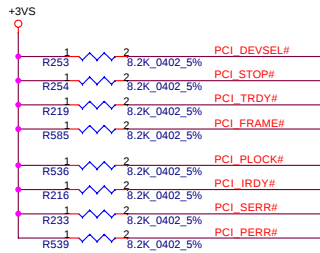
DSUB



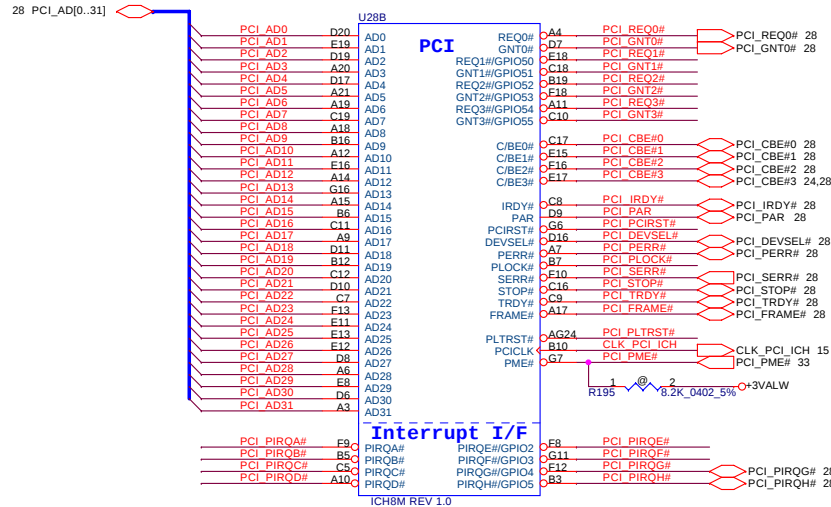
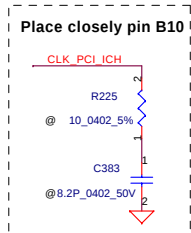
PIN ASSIGMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYS			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

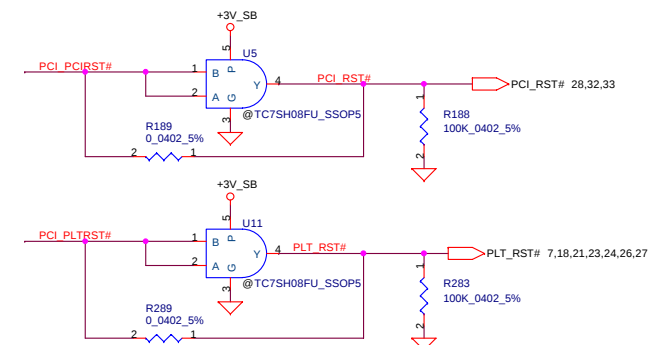
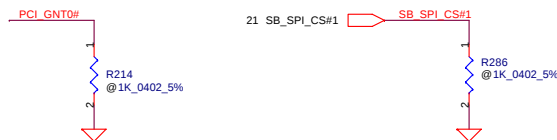




A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

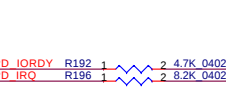
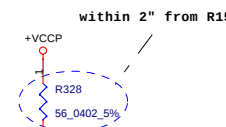
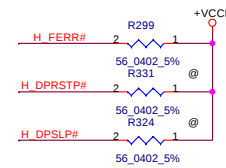
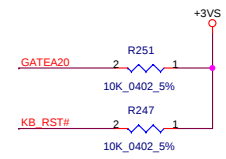


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_INTVRMEN	



+3VS
R543 2 1 HDA_SDOUT AUDIO
@1K_0402_5%

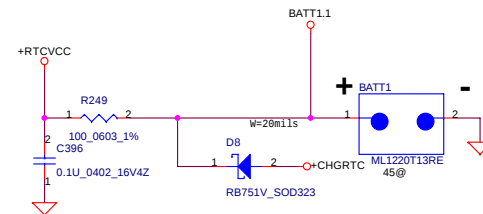
29 HDA_SDOUT_AUDIO 1 R548 2 33_0402_5% HDA_SDOUT_R

29 HDA_SYNC_AUDIO 1 R557 2 33_0402_5% HDA_SYNC_R

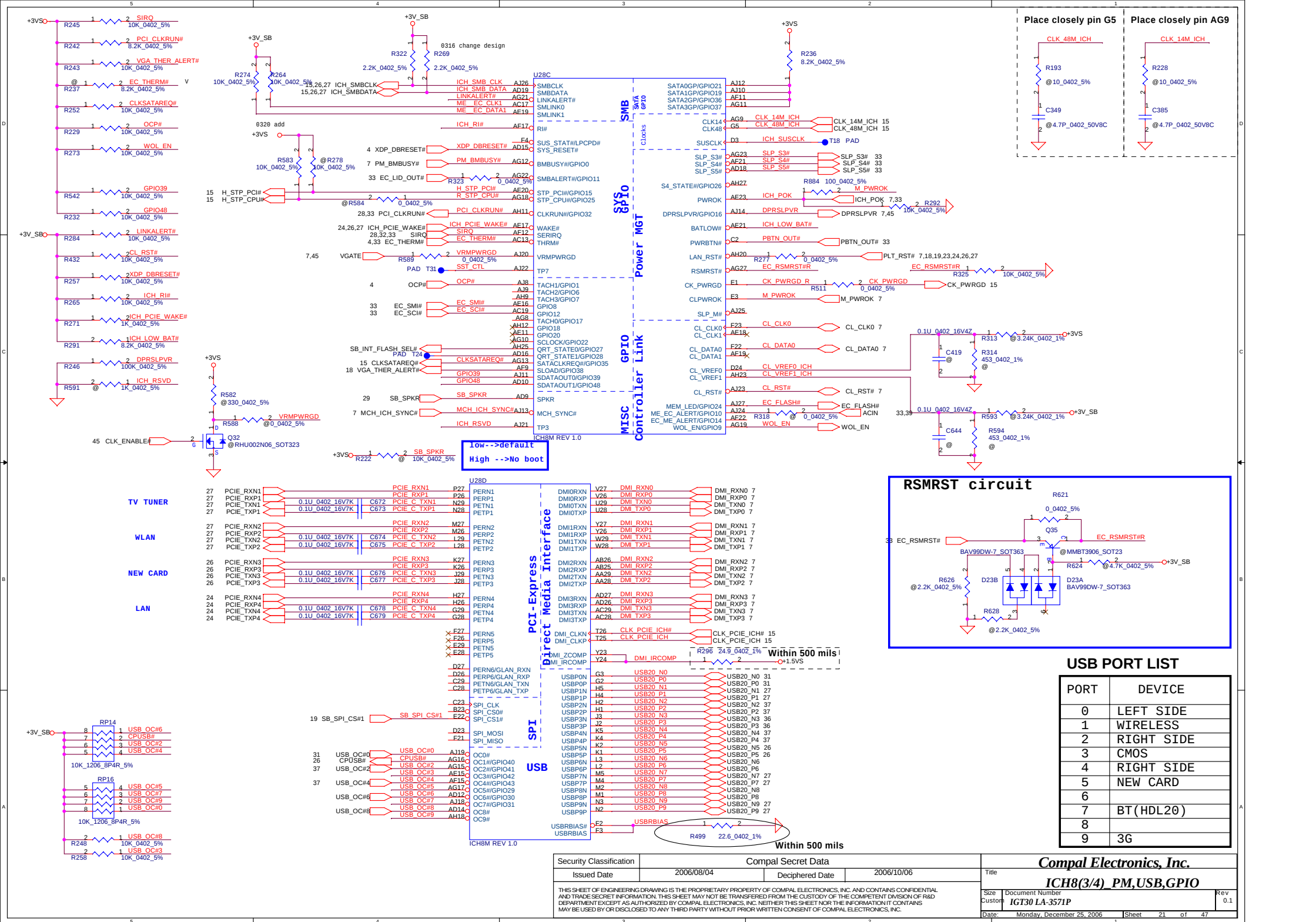
29 HDA_RST_AUDIO# 1 R553 2 33_0402_5% HDA_RST_R#

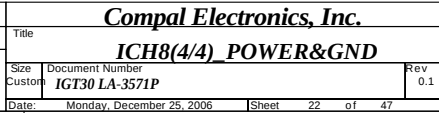
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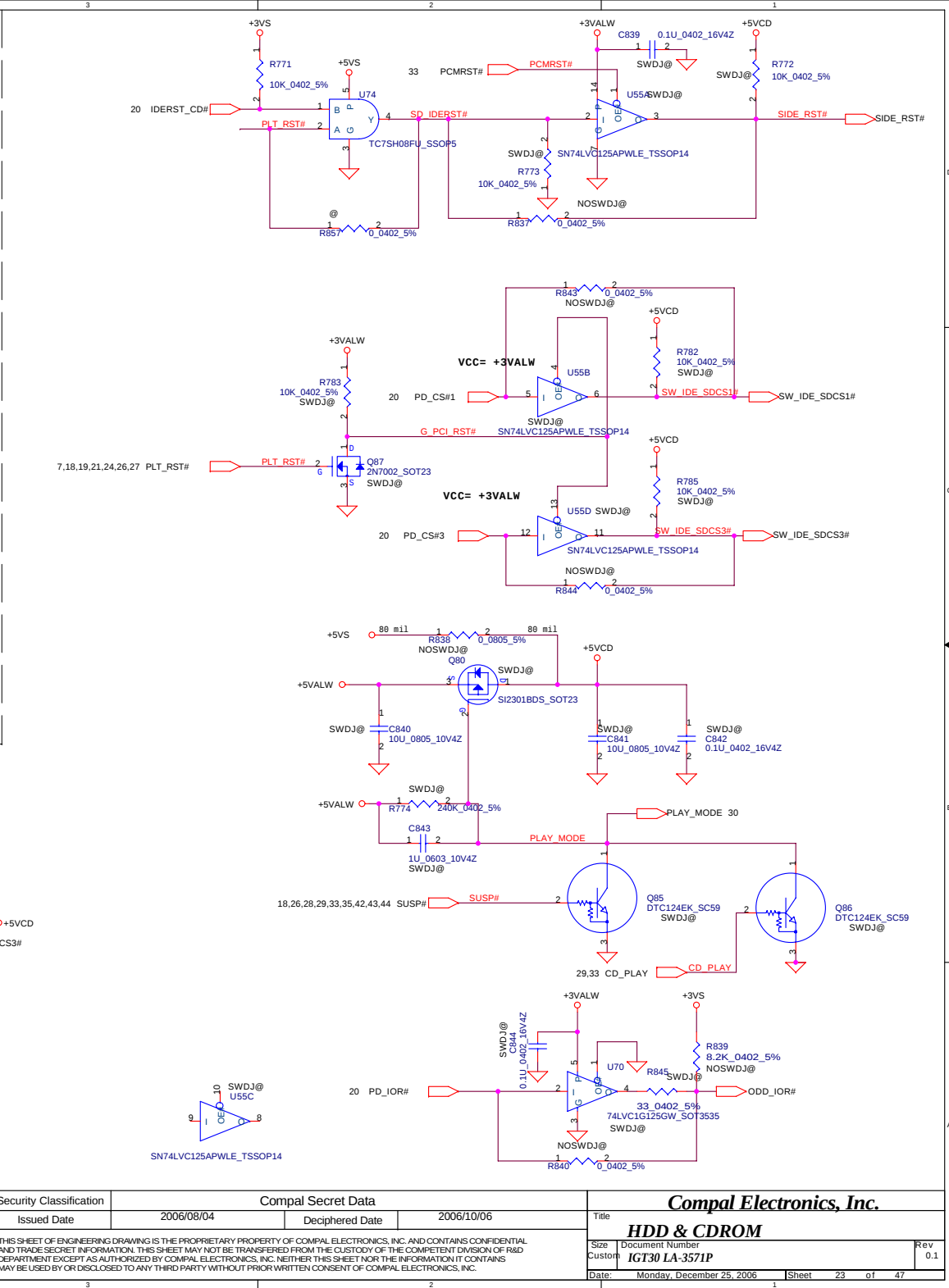
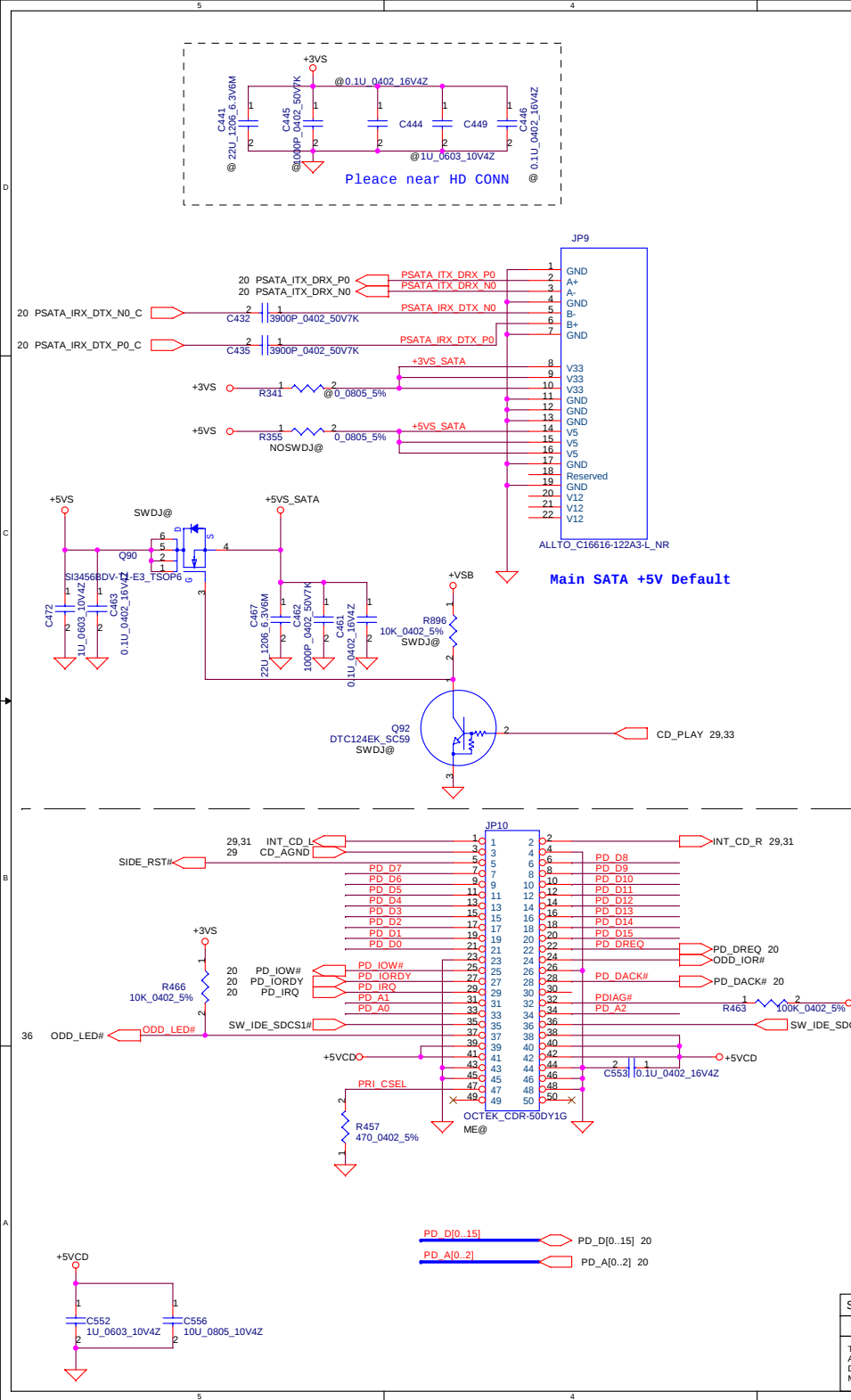
@C394
27P_0402_50V8J



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						Date	Monday, December 25, 2006
						Sheet	23 of 47

Compal Electronics, Inc.

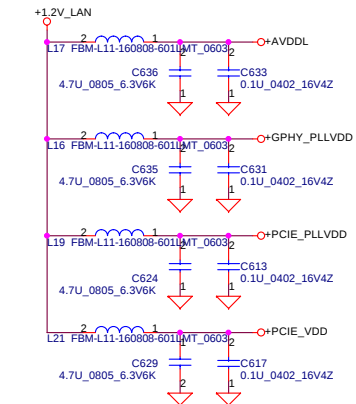
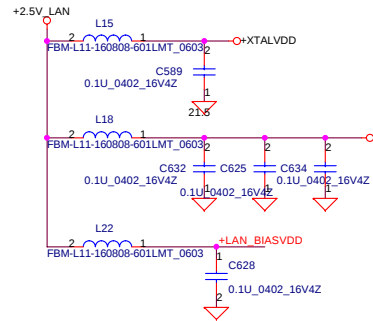
HDD & CDROM

Rev 0.1

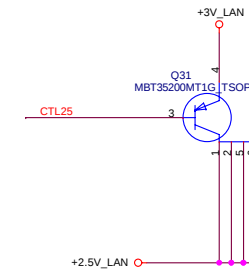
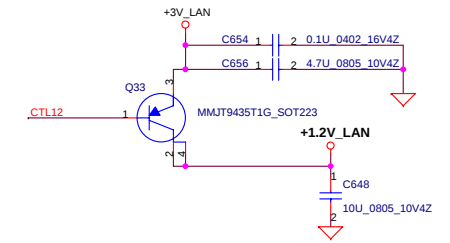
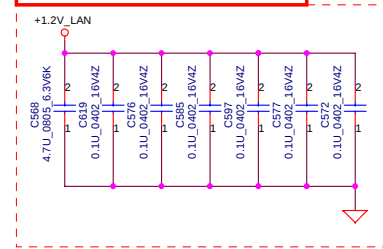
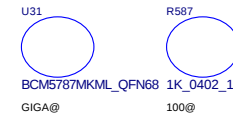
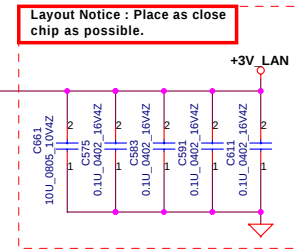
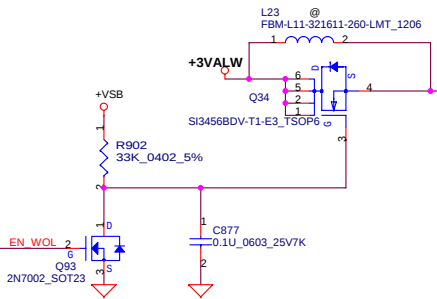
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

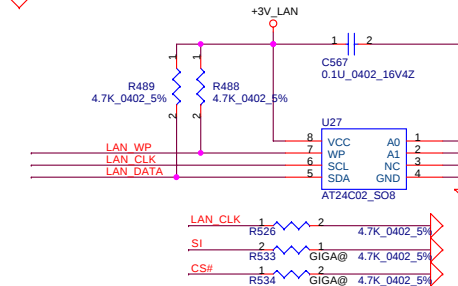
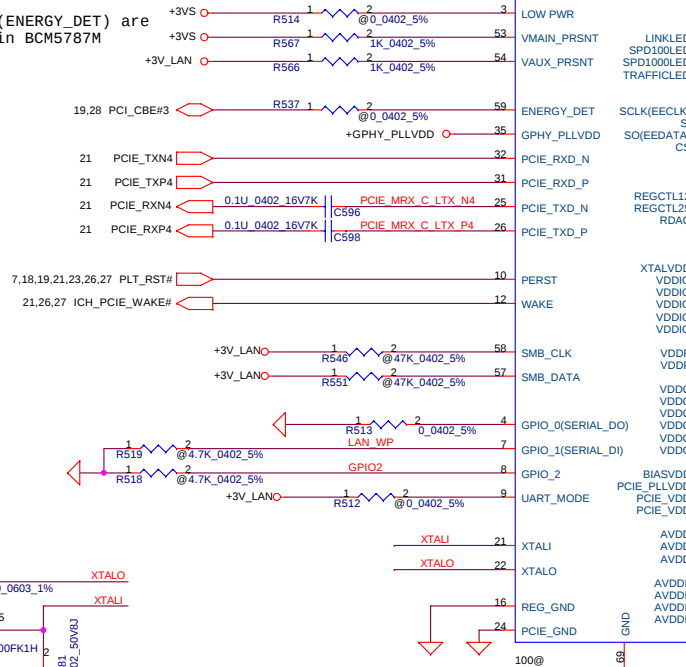
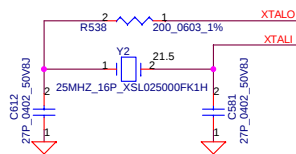
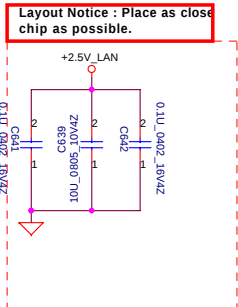


(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

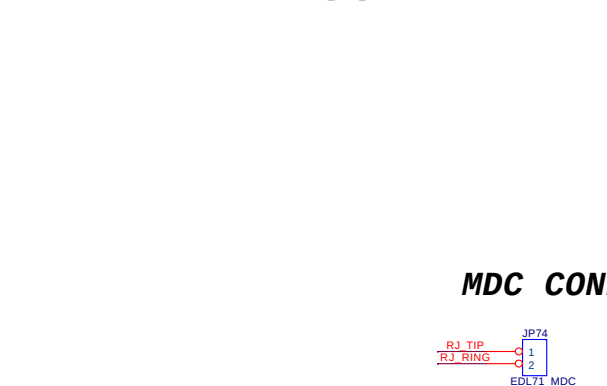
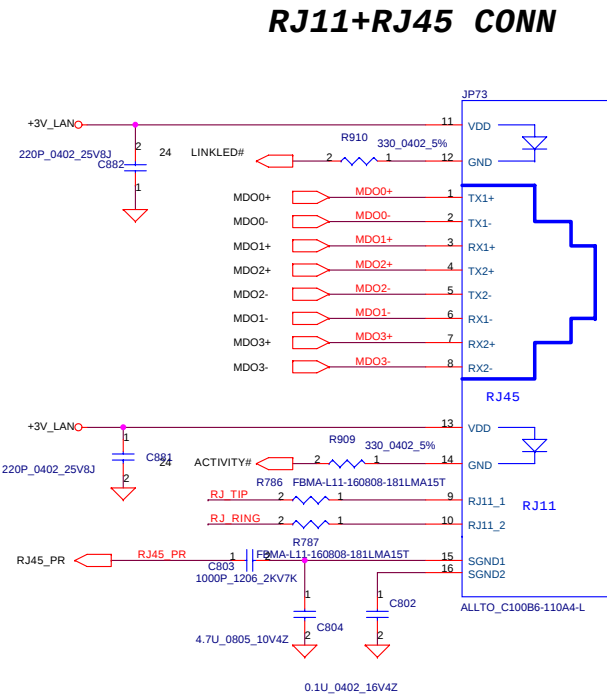
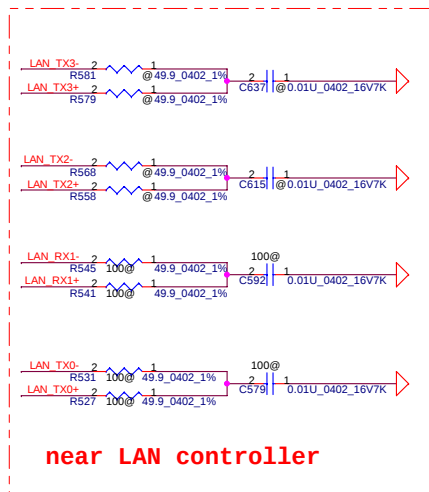
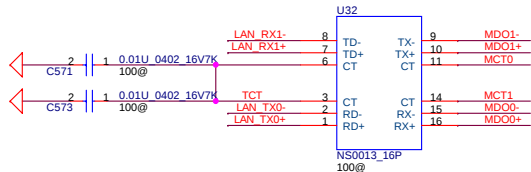
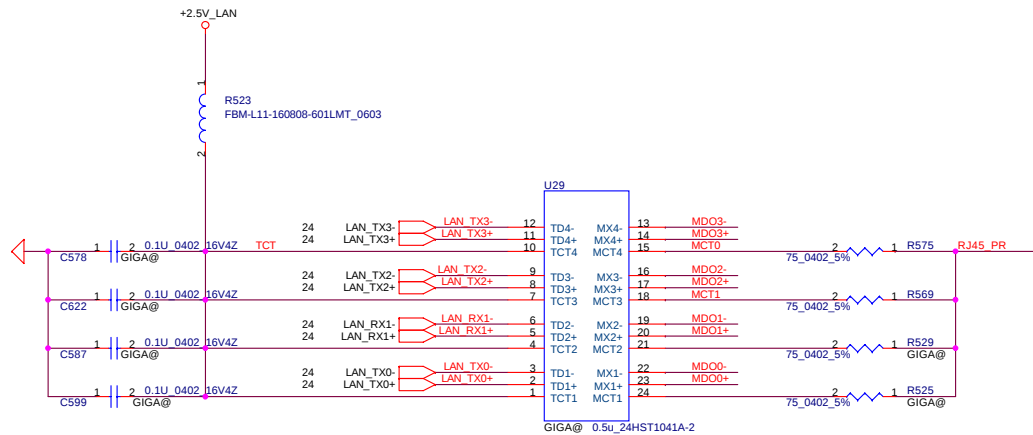


Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.



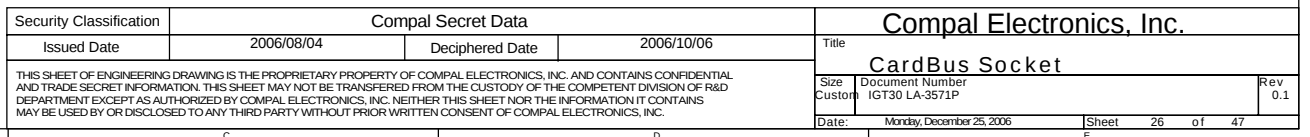
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title		
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				Size	Document Number	Rev
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				Size	Document Number
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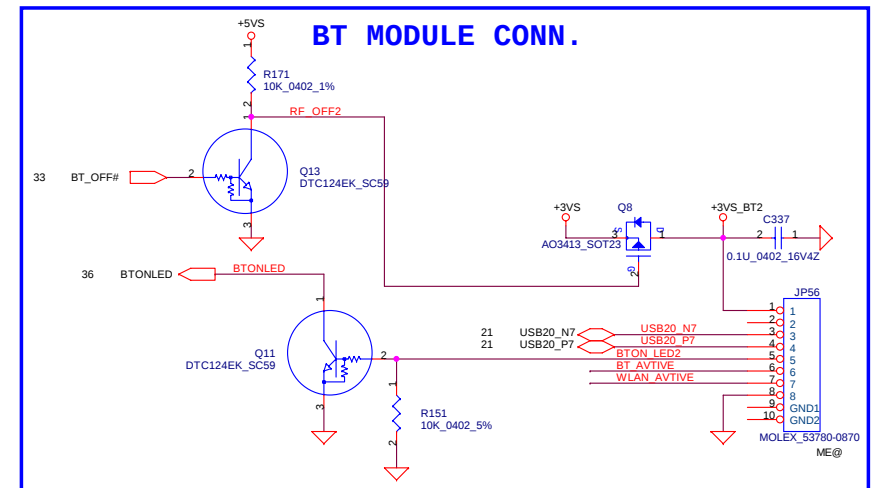
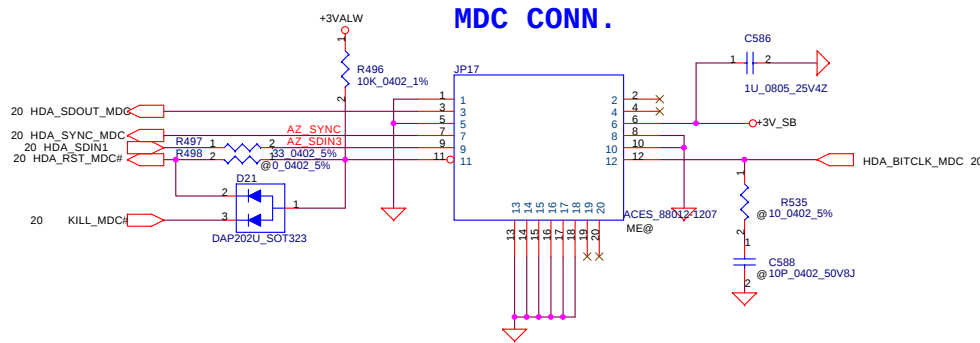
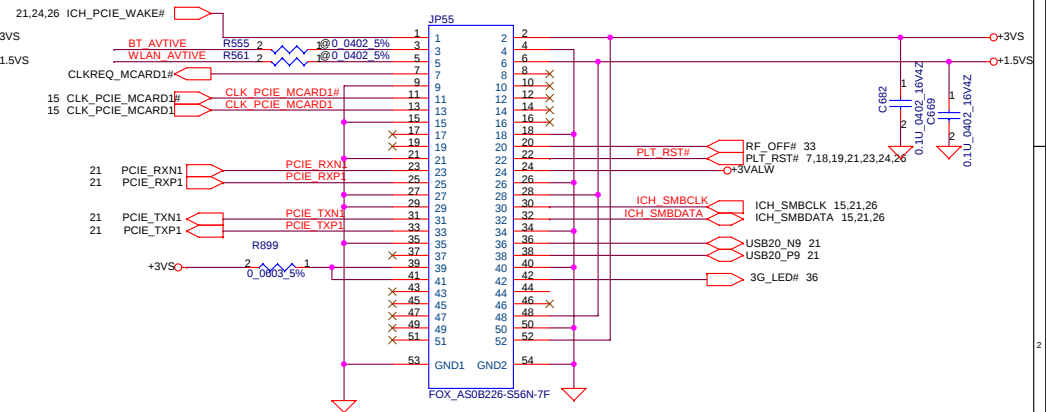
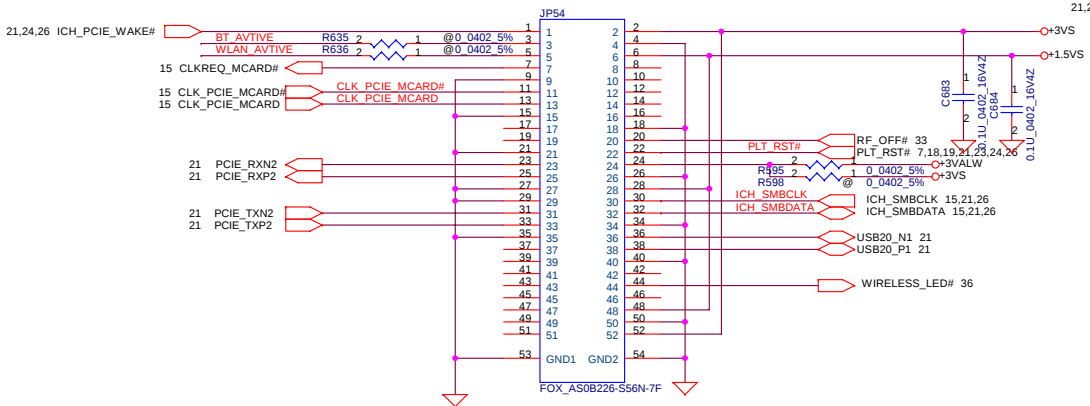
Express Card Power Switch

The schematic diagram illustrates the power switch circuit for an Express Card. The central component is the U8 power switch IC (R5538_QFN20). The circuit is powered by +1.5V_S0 and +3V_S0, which are filtered by capacitors C378 and C375. The +3V_S0 is also filtered by C389. The +3V_S0 is connected to the +3VALW0 pin of the U8. The U8 provides outputs for 1.5V_Sin, 1.5V_Sout, 3.3V_Sin, 3.3V_Sout, AUX_IN, AUX_OUT, SYSRST#, SHDN#, STBY#, CPPE#, CPUSB#, and RCLKEN. The circuit also includes several capacitors (C373, C365, C384, C392, C371) and resistors (R211, R212) for filtering and signal conditioning. The output of the switch is connected to the Express Card's power pins.

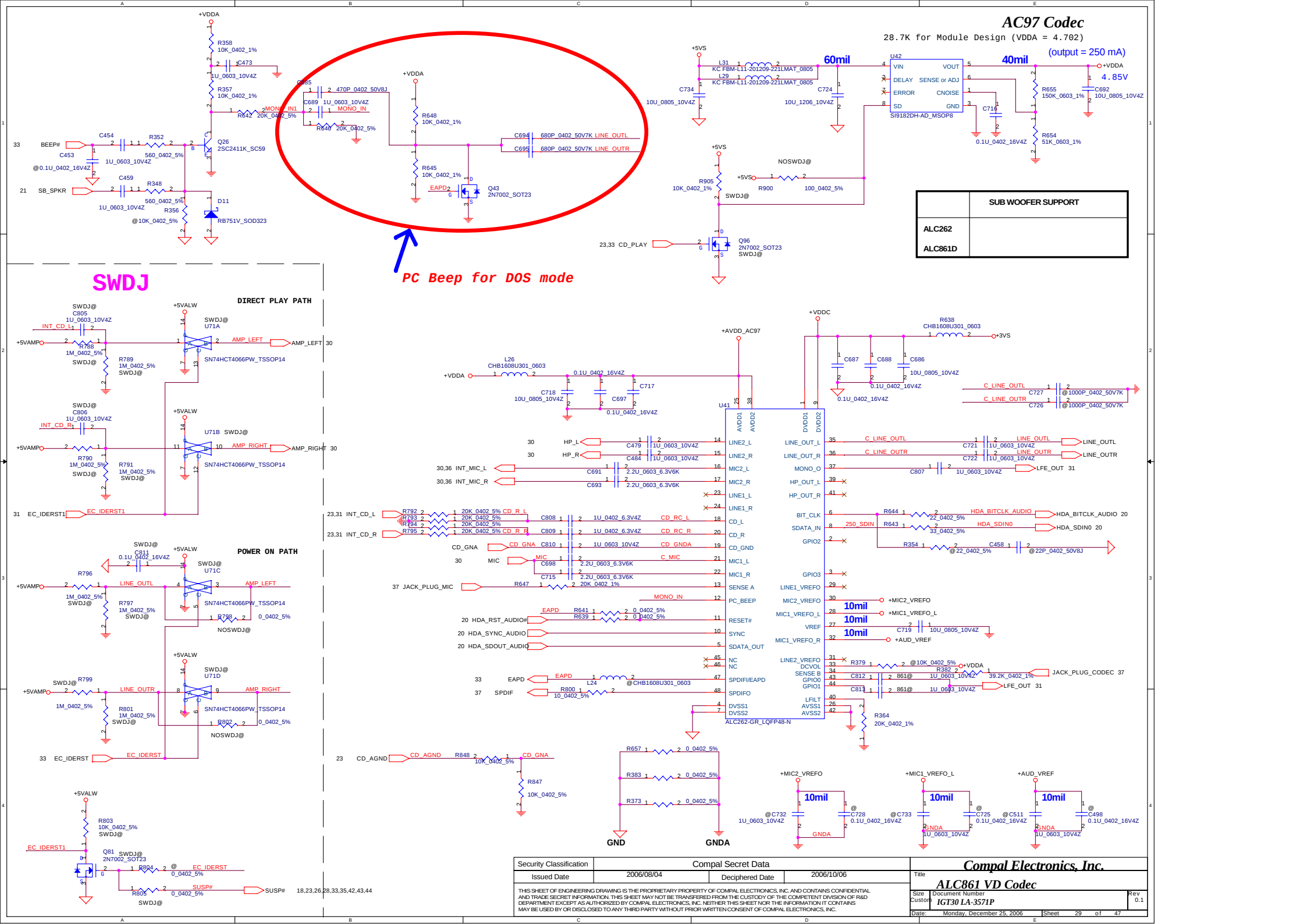


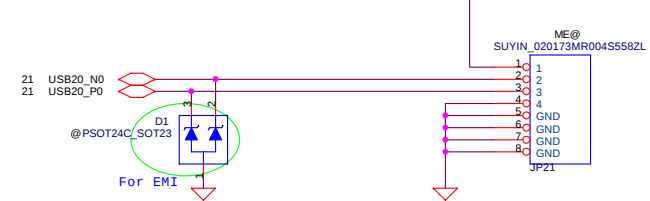
Mini-Express Card(Slot 1-WLAN)

Mini-Express Card(Slot 2-3G)

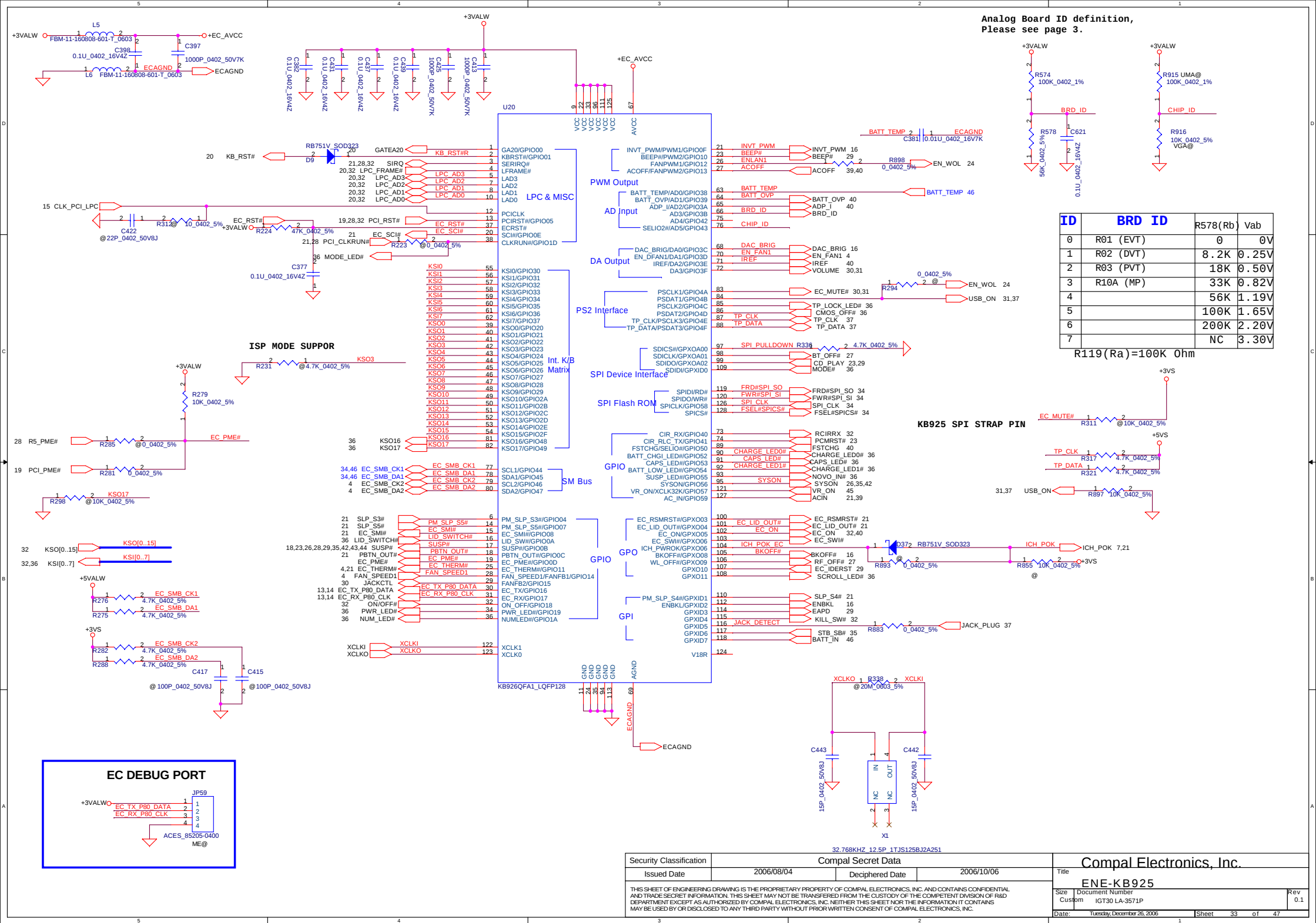


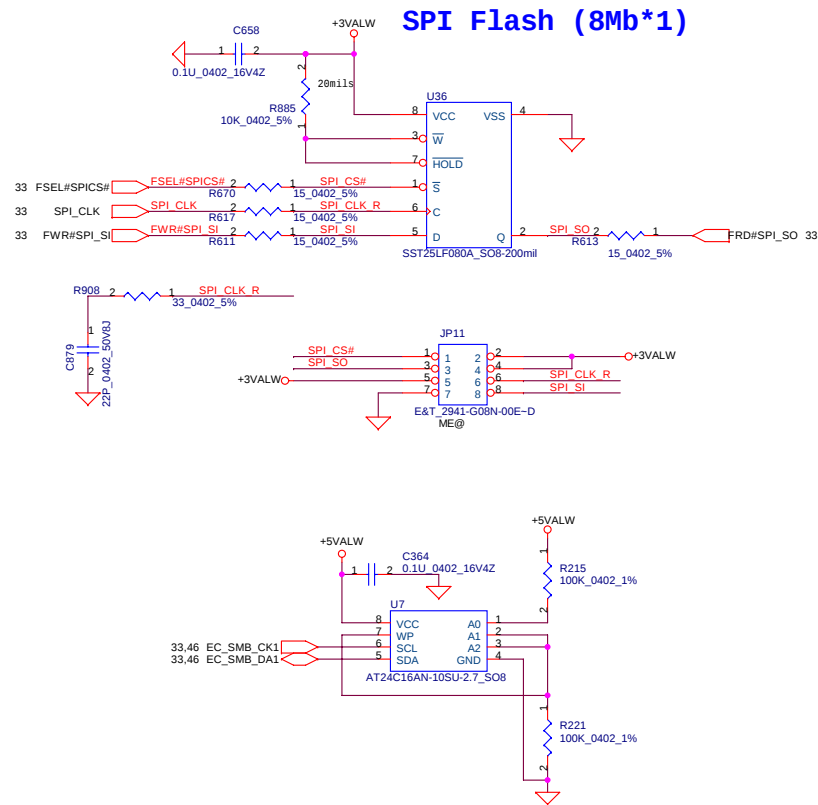
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Size	Document Number	Rev		0.1	
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Date	Monday, December 25, 2006	Sheet	27	of 47	



WOOFER@

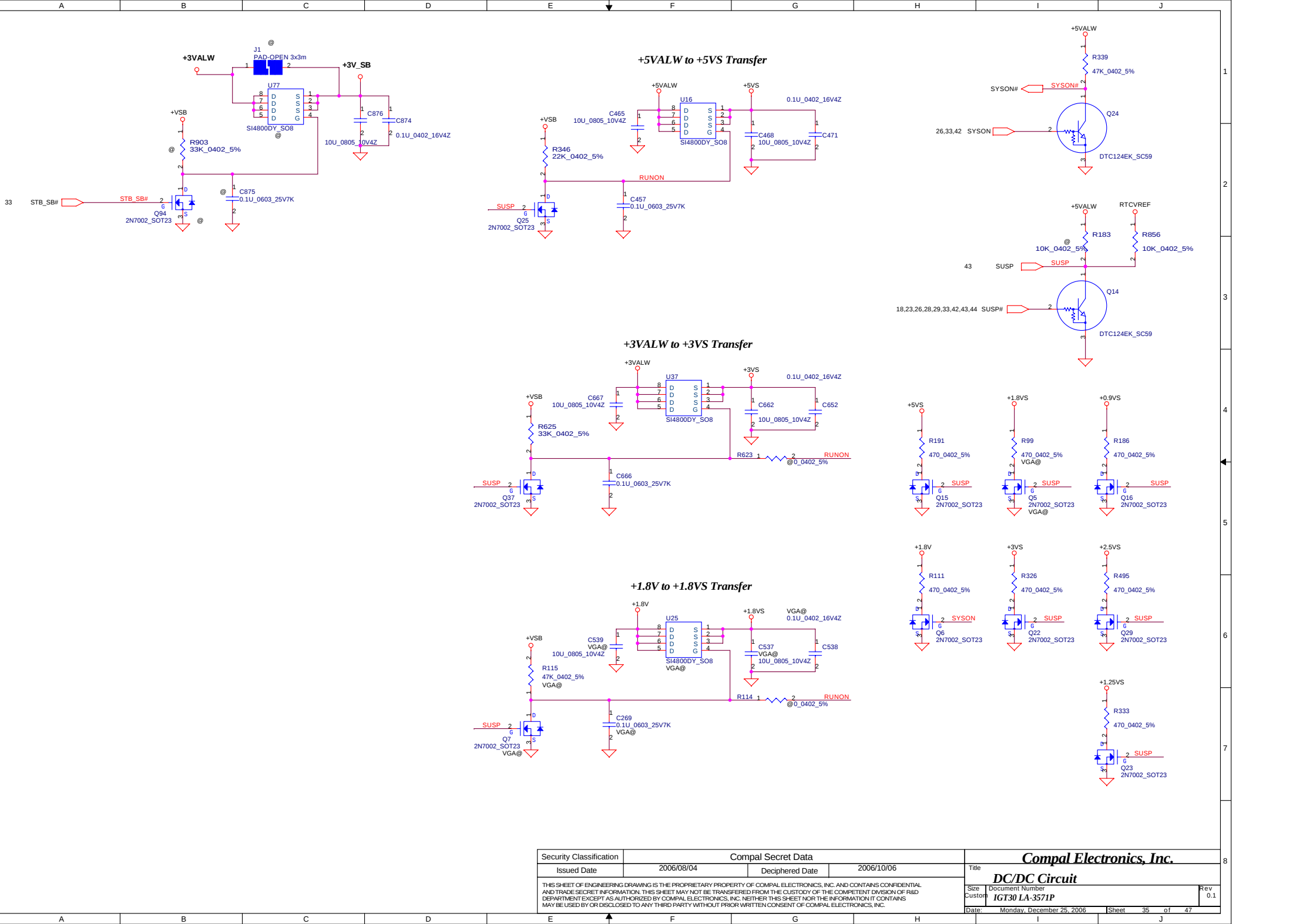
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				Size		Document Number		Rev	
				Date		IGT30 LA-3571P		0.1	
		Tuesday, December 26, 2006		Sheet		31 of 47			



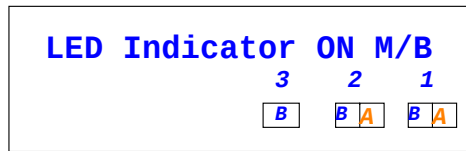


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										Size	
										Document Number	
										IGT30 LA-3571P	
										Rev	
										0.1	
										Date:	
										Monday, December 25, 2006	
										Sheet	
										34	
										of	
										47	

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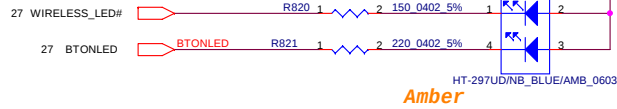


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Wireless / Bluetooth LED

Blue



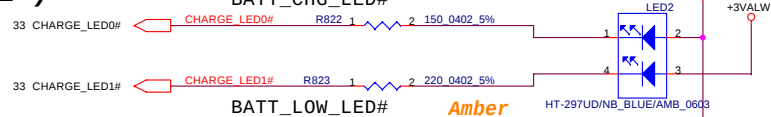
STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Amber

(2)

BATT_CHG_LED#

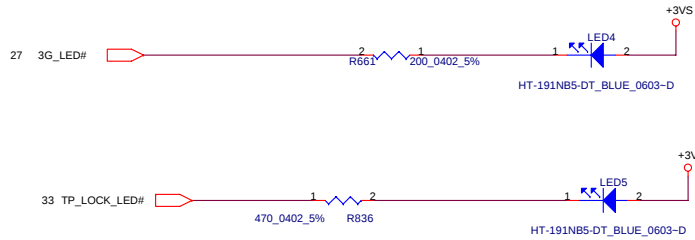
Blue



Amber

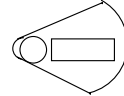
(3)

Blue : Power On,
Blinking Blue : Suspend



STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Dial Wheel

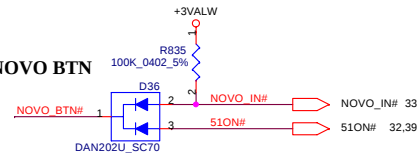


Function

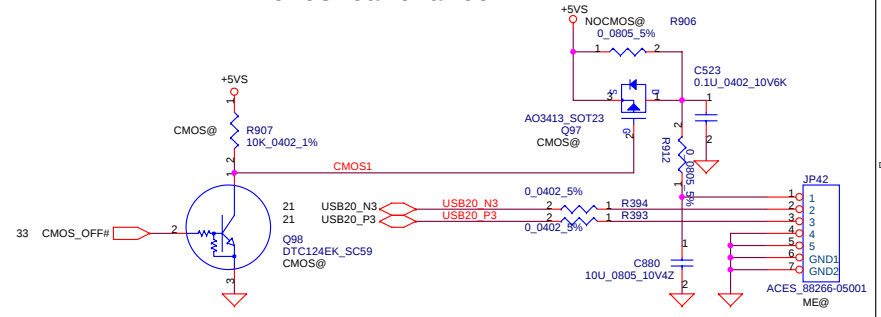
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KSI0	DW-UP	DW-DOWN
KSI1	DW-ENTER	MUTE

NOVA_BTN#

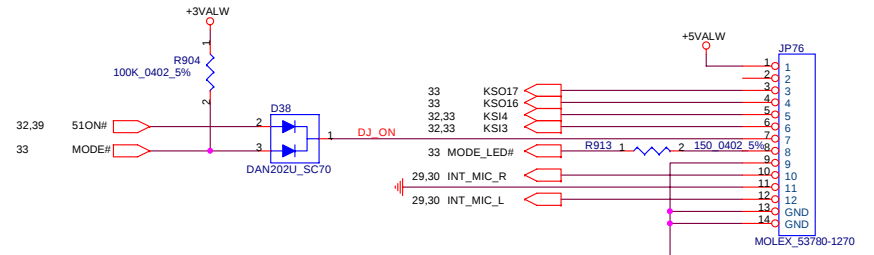
NOVO BTN



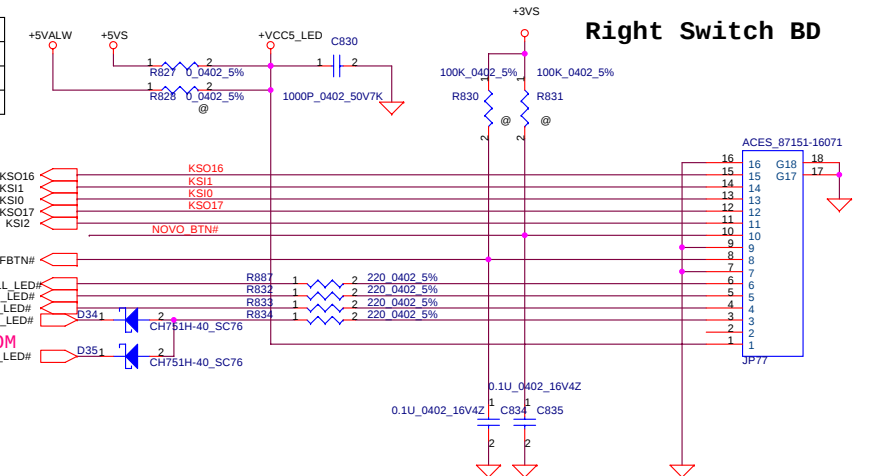
CMOS Camera Conn



Left Switch BD(AUDIO DJ)



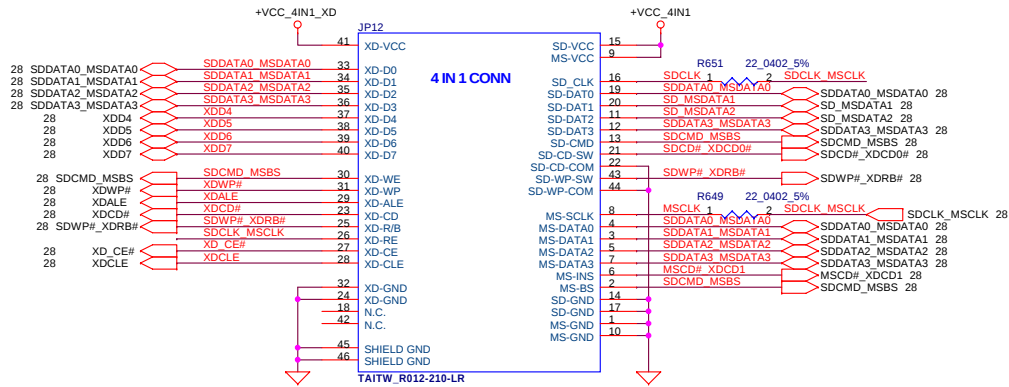
Right Switch BD



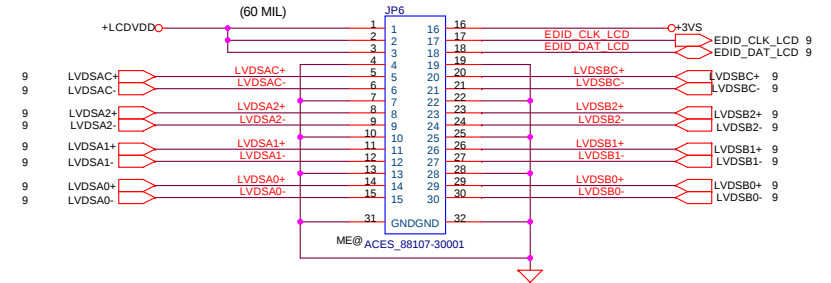
C839, C841, C842 For EMI Solution

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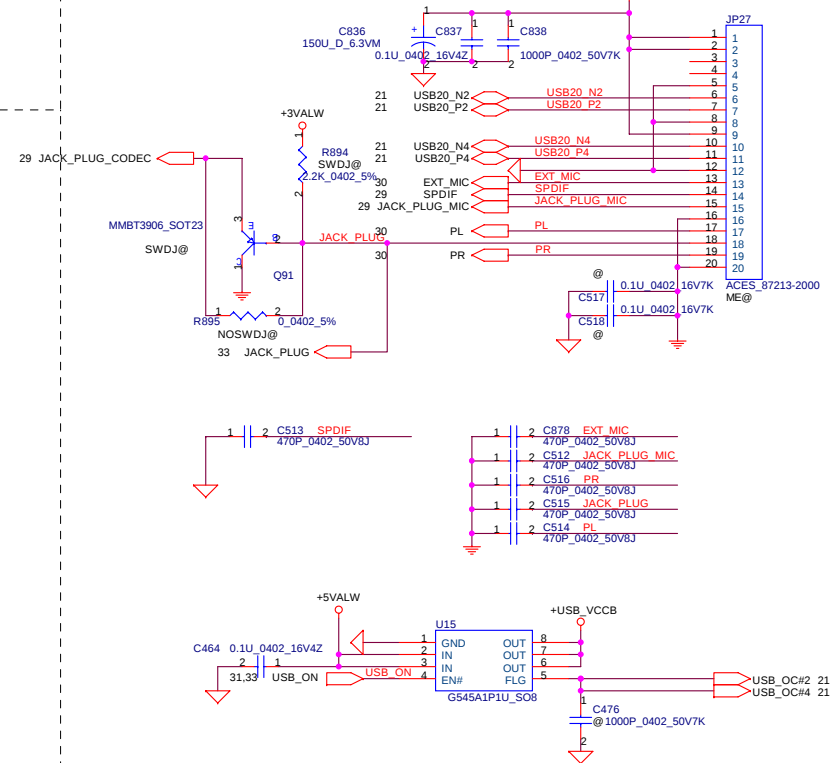
4 in 1 Card Reader



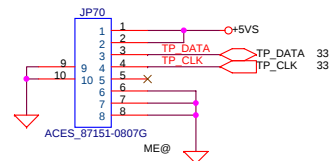
UMA LCD/PANEL Conn.



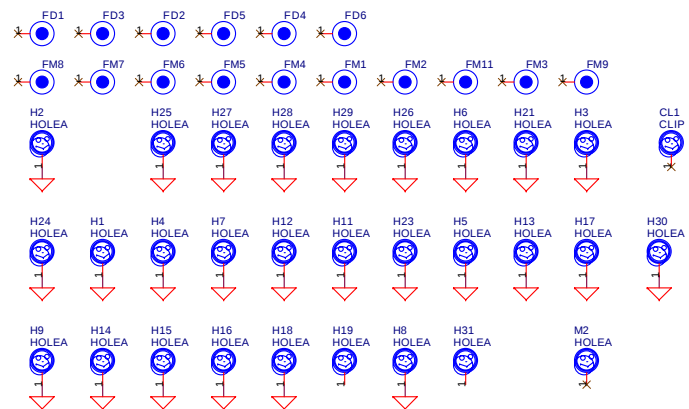
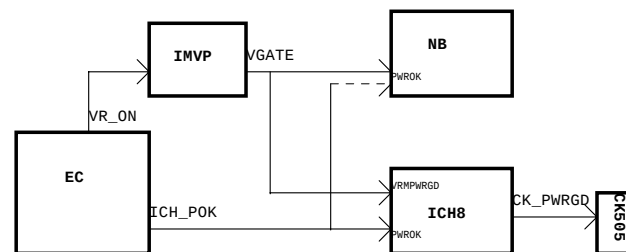
Audio Jack/USB Conn.



T/P Board



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						IGT30 LA-3571P					0.1
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ACIN

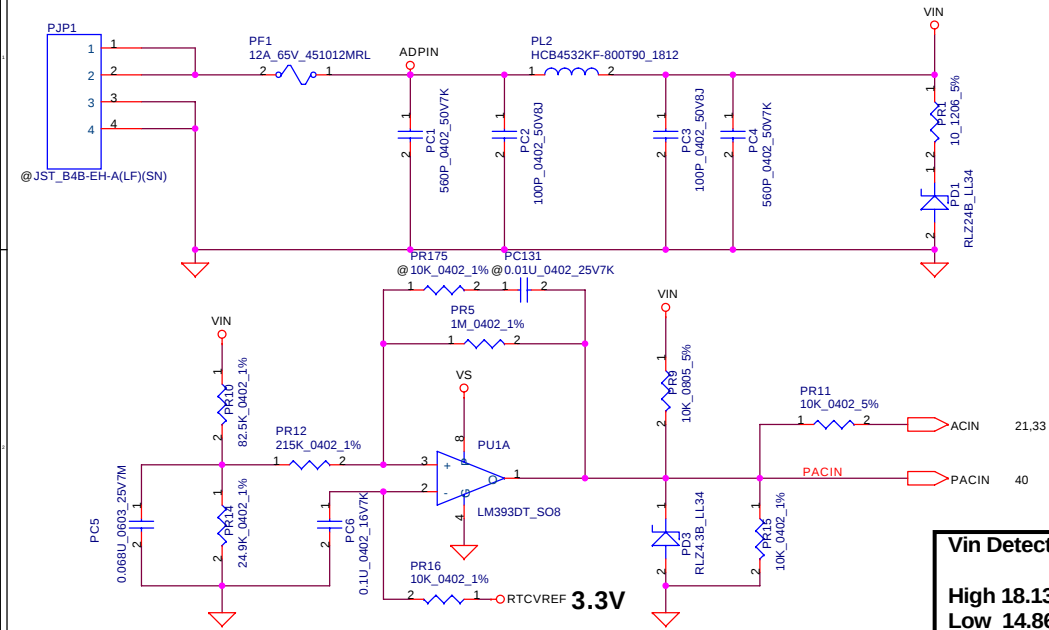
Precharge detector

	Min.	typ.	Max.
H-->L	13.843V	14.247V	14.636V
L-->H	14.936V	15.381V	15.814V

BATT ONLY

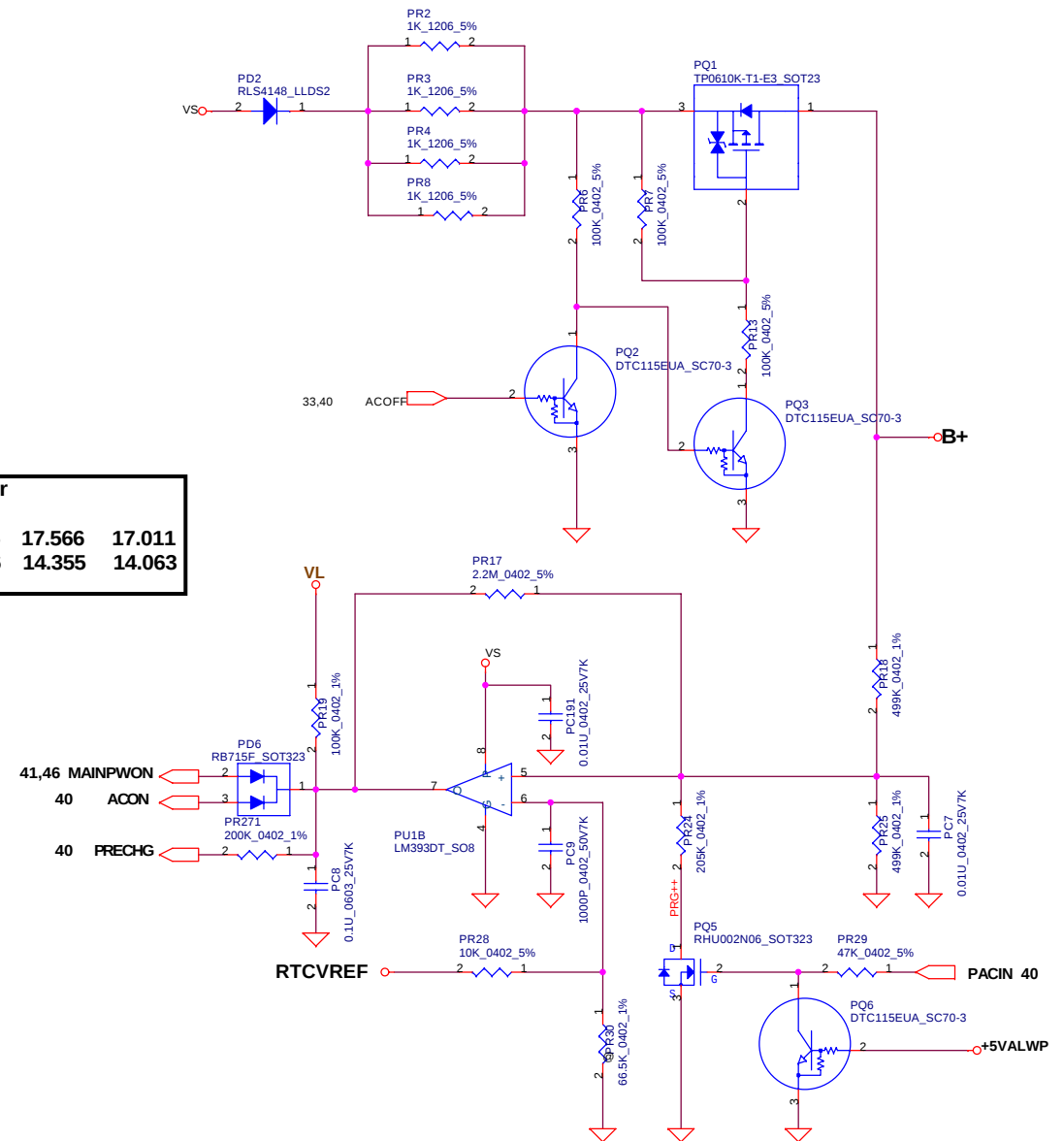
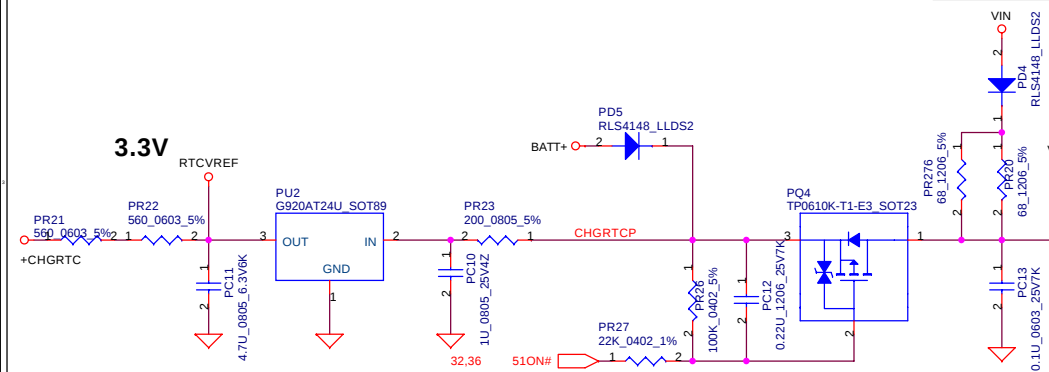
Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

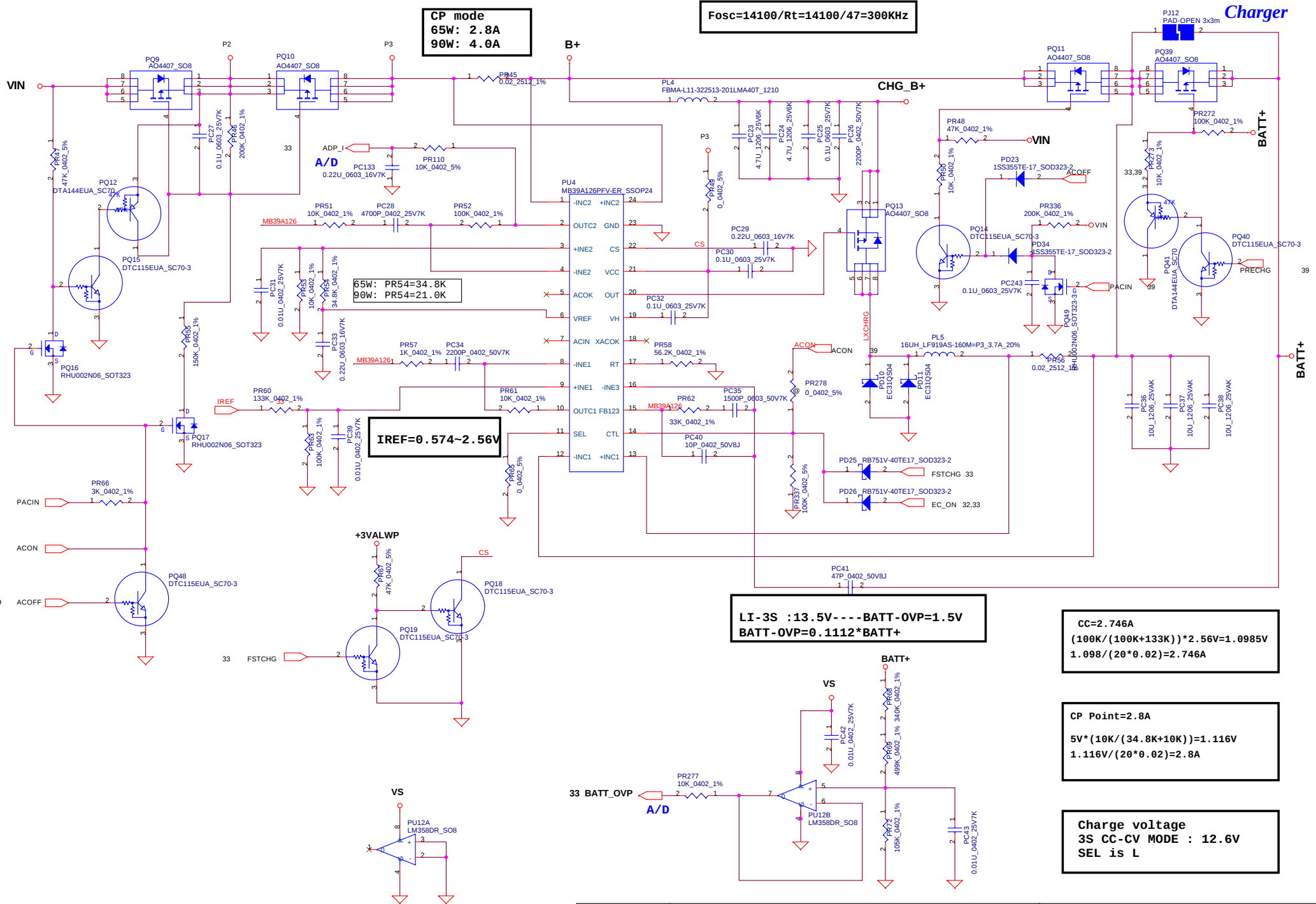


Vin Detector

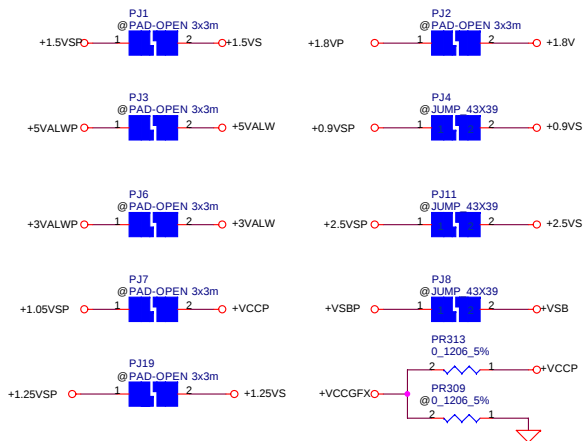
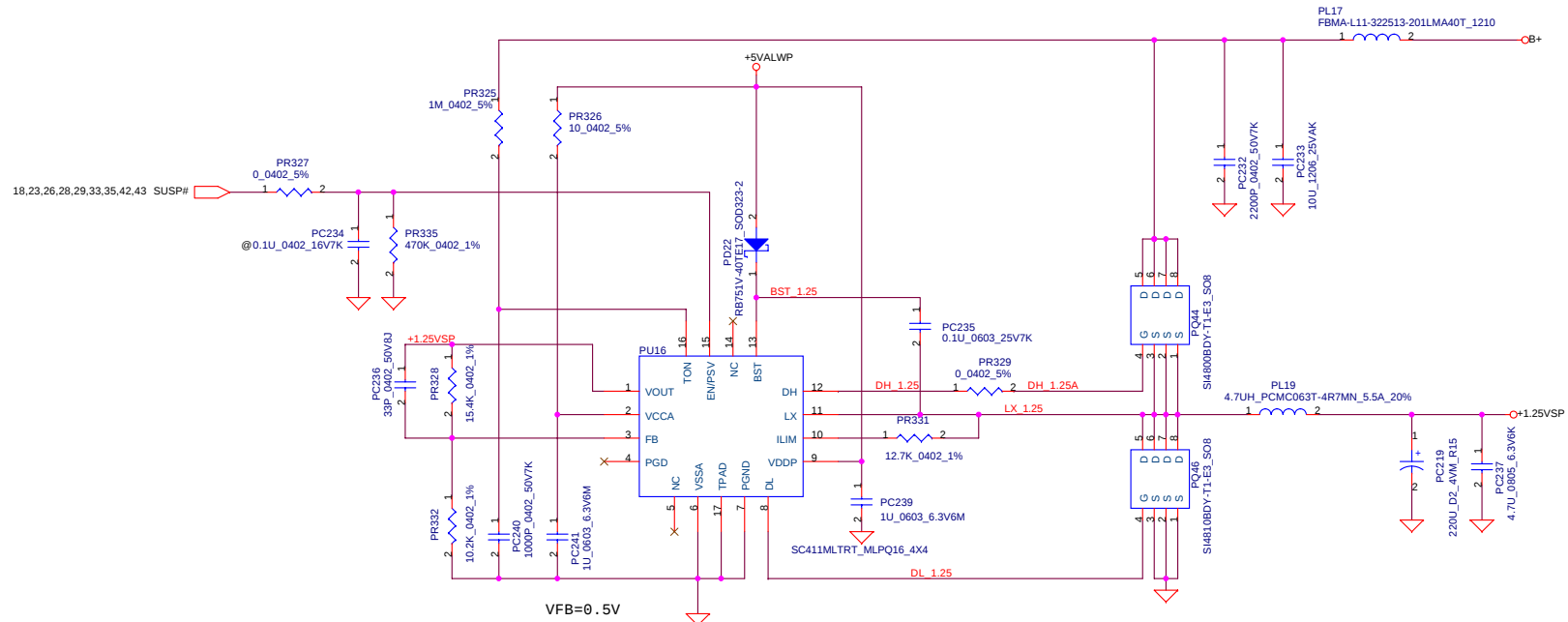
High	18.135	17.566	17.011
Low	14.866	14.355	14.063



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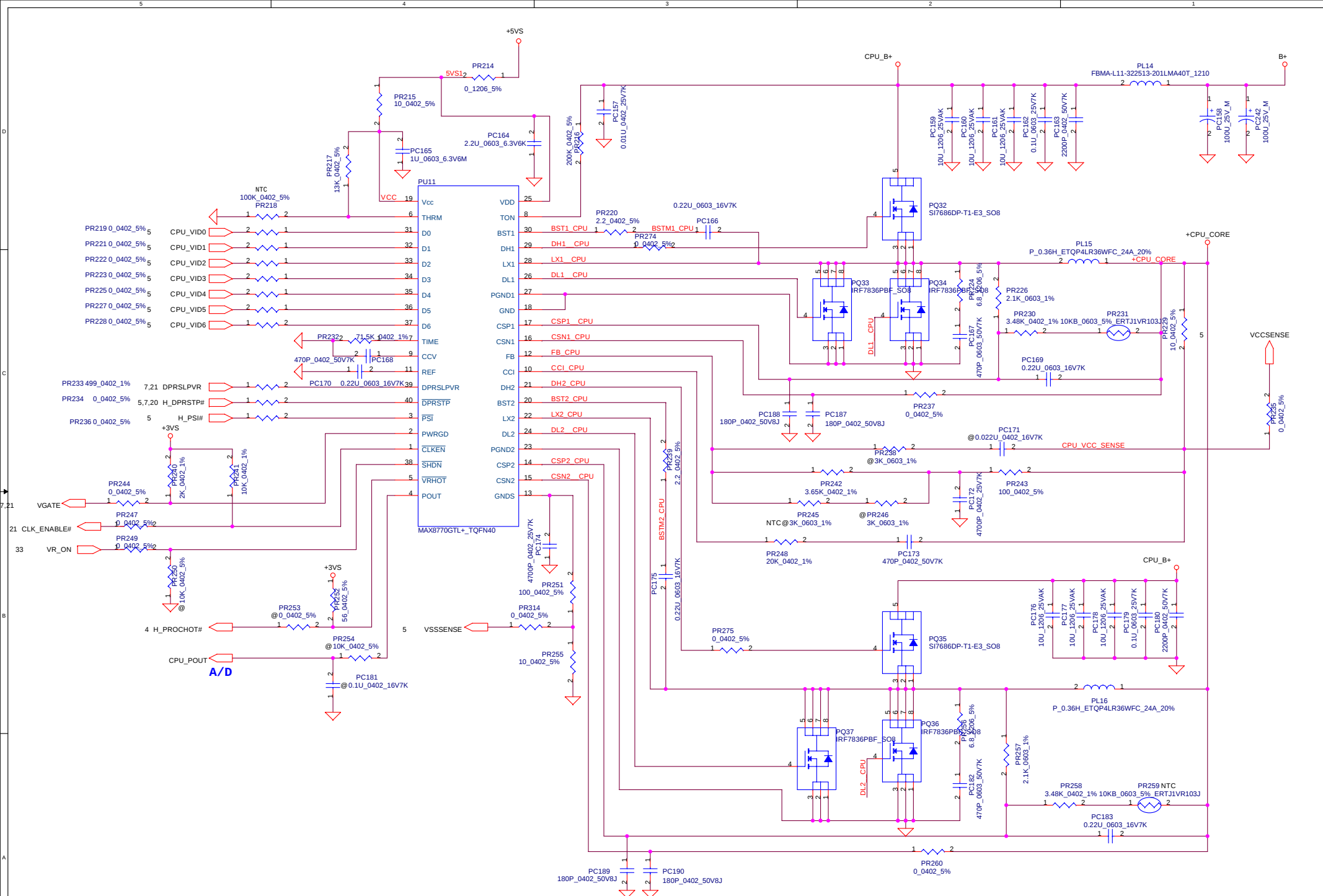


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